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An analytical analysis of Quantum capacitance in nano-scale Single-wall Carbon Nano Tube Field Effect Transistor (CNTFET)

Ajay Kumar Singh

Faculty of Engineering and Technology-Multimedia University- Melaka Malaysia

*aks_1993@yahoo.co.uk/ajay.singh@mmu.edu.my

Abstract

This paper discusses the quantum capacitance effect in single-wall conventional CNTFET devices. The analytical expression for quantum capacitance has been derived based on the normalized number of carriers/ total charge density. The total charge density in the inverted channel is suppressed at large drain voltage but remains unaffected by introducing any new sub-band. Lowering the quantum capacitance in the CNTFET device is a major challenge to improve the performance of the device. Quantum capacitance takes lower value at higher sub-band when operated at low gate bias voltage. Lower quantum capacitance can be achieved for larger tube's diameter due to reduced band gap and by controlling the BTBT (band-to-band tunneling) leakage current which is possible by choosing the proper dielectric material and gate oxide thickness.

[Key words: Carbon nano tube, Density of States, Gate capacitance, Quantum capacitance, Total charge density]

I. Introduction

Single-wall carbon nanotube field effect transistor (CNTFET) is future candidate to replace conventional Si-MOSFET due to better control of the short channel effects (SCEs) in nano scale regime [1-4]. CNTs are graphite sheets in the shape of tube and can be classified as metallic or semiconductor depending on the direction in which the nanotubes are rolled (Figure 1(a)) [5-6]. The semiconductor nanotubes are mainly used in the design of high performance transistors where channel is the tube itself (Figure 1(b)) [7-9]. There has been immense research carried out by researchers to understand the electrical behavior of CNTFETs [10-12]. The various capacitances in CNTFET devices are shown in Figure 1(c), where C_g is total capacitance between channel and gate, C_S and C_D are the parasitic capacitances in the channel at the source/drain end respectively [13]. From the circuit's point of view, it is necessary to study capacitance C_g which is expressed as the series combination of gate oxide capacitance (C_{ox}) and inversion layer capacitance ($C_{inv.}$) (Figure 1(d)) [14-15]. The inversion layer capacitance is represented by the series combination of quantum capacitance (Cq) and electrostatic capacitance for only one occupied sub-band. Quantum capacitance (C_q) is a consequence of Pauli Exclusion Principle

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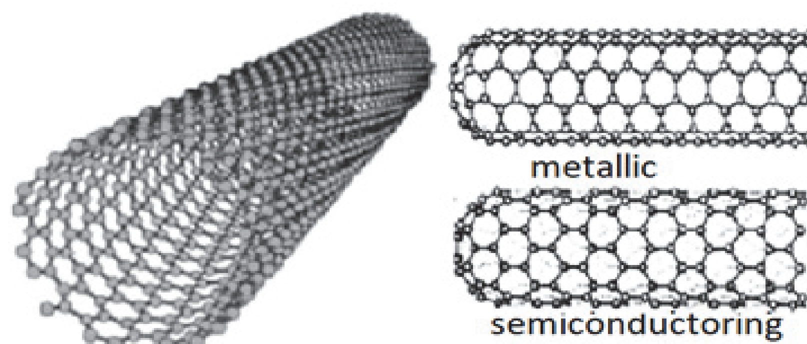
which requires an extra energy to fill the quantum well with electrons and was first introduced by S. Luryi [16]. C_q is bias dependent and associated with channel material. For nanometer oxide thickness, C_{ox} approaches to the inversion capacitor (Figure 1(d)) and hence in this situation quantum capacitance starts to affect the total capacitance of the device. Effect of quantum capacitance is quite prominent in the case of CNTFET devices due to relatively low density of state (DOS). Researchers have studied the quantum capacitance in CNTFET [17-20] in detail but no proper analytical expression is available in the literature.



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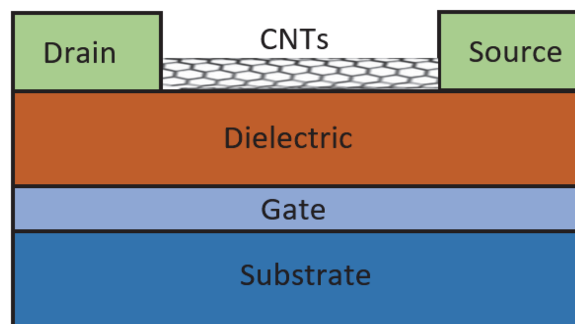

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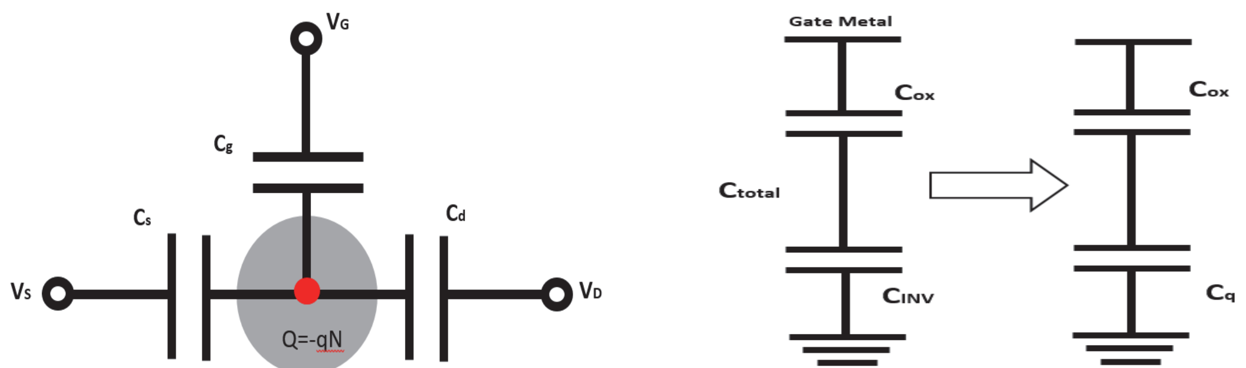

(c) (d)

Figure 1: (a) Structure and type for CNTs [6] (b) Structure of semiconductor nanotube [7] (c) Various capacitances in CNTFETs [13] (d) Total gate capacitance in CNTFETs [14]

In this present paper, we have analyzed the quantum capacitance in the single-wall CNTFET device after proposing an analytical expression based on carrier charge density. The analytical expression shows that Cq depends on the bias voltage and oxide/channel material. We have observed that the total charge density in the channel is suppressed in the inversion region at large drain voltage whereas it does not show any variation with gate voltage. In subthreshold region, C_q remains insensitive to the change in drain voltage but decreases with gate voltage due to negligible quantization effect. The performance of the CNTFET devices can be improved by reducing the quantum capacitance which can be achieved by increasing the tube's diameter or choosing the gate material of higher dielectric permittivity. The rest of the paper is organized as follows; section II describes the analytical expressions of total charge density and quantum capacitance. Section III discusses the simulation results and section IV concludes the paper.

II. Analytical Models

Quantum capacitance (C_q) physically originates from the penetration of the Fermi-level (E_F) into conduction band. In carbon nanotube field effect transistor (CNTFET), quantum capacitance needs to be considered because Cq is comparable to the oxide capacitance (C_{ox}) and defined as [18];

$$Cq = \frac{dQcnt}{dVa} \tag{1}$$

Where Va is applied local potential and Qcnt is charge density which is given as;

$$Qcnt = q\sum_p n_{CNT} \tag{2}$$

n_{CNT} is the number of carriers in the pth sub-band [21];

$$n_{CNT} = \int_0^\infty D_{CNT}\left(\frac{E-E_0}{2}\right) f\left(E - E_0 - E_{F_i}\right) dE \tag{3}$$

E_0 is mid band gap (=qV_{CNT}+ deltap), deltap is equilibrium conduction band minima of the pth sub-band, V_{CNT} is modulated potential in the channel due to gate bias voltage, D_{CNT} is the density of states (DOS) and given as [21];

$$D_{CNT} = \frac{N_0(E - qV_{CNT} + deltap)}{\sqrt{(E - qV_{CNT} + deltap^2) - (deltap)^2}} \tag{4}$$

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$N_0 = \frac{4}{3}\frac{1}{(\frac{V_p}{KT})b}$, V_p is carbon-carbon bond energy (=3 ev) and b is carbon-carbon bond distance (=0.142 nm) and $f(E-E_0-E_{Fi})$ is Fermi-Dirac statistics.

The charge at the top of the barriers is controlled from source as well as drain. All the +k-states at the bottom of the top is occupied by source while –k states are filled by the drain and hence equation (3) is rewritten as;

$$n_{CNT} = \left(\frac{N_0}{2}\right)[\int_0^{\infty} \frac{(E-qV_{CNT}+deltap)}{\sqrt{(E-qV_{CNT}+deltap)^2)-(deltap)^2}} \left\{\frac{1}{1+e^{(\frac{E-qV_{CNT}+deltap-E_{F_S}}{KT})}} + \frac{1}{1+e^{(\frac{E-qV_{CNT}+deltap-E_{F_D}}{KT})}}\right\} dE] \quad (5)$$

$E_{Fs}(E_{FD})$ is the source(drain) Fermi-Level. After assuming, E_{Fs}=qvgs and E_{FD}=qvds, equation (5) can be written as;

$$n_{CNT} = \left(\frac{N_0}{2}\right)[\int_0^{\infty} \frac{(E-qV_{CNT}+deltap)}{\sqrt{(E-qV_{CNT}+deltap)^2)-(\Delta p)^2}} \left\{\frac{1}{1+ e^{(\frac{E-qV_{CNT}+deltap-qv_{gs}}{KT})}} + \frac{1}{1+e^{(\frac{E-qV_{CNT}+deltap+qv_{ds}}{KT})}}\right\} dE] \quad (6)$$

Expressing the gate-source and drain-source voltages in terms of applied voltage Va as; Va=vds-V_{CNT} at the drain end and Va=vgs+V_{CNT} at the source end, and assuming $(\frac{E+deltap\pm qV_a}{KT}) \gg 1$, equation (6) reduces to;

$$n_{CNT} = \left(\frac{N_0}{2}\right)\cosh\left(\frac{Va}{V_t}\right)[\int_0^{\infty} \frac{1}{\sqrt{(1)-(\frac{deltap}{E-qV_{CNT}-deltap})^2}} \left\{e^{-(\frac{E+deltap}{KT})}\right\} dE] \quad (7)$$

After performing the integration, we get;

$$n_{CNT} = \left(\frac{N_0}{2}\right)\cosh\left(\frac{Va}{V_t}\right)e^{-(\frac{V_{CNT}}{v_t})}[+(\frac{deltap}{KT\sqrt{2}})^2\{E_i(beta) - \left(\frac{1}{beta}\right)e^{-beta}] \quad (8)$$

Where, E_i(beta) is the exponential integration factor and $beta = \frac{qV_{CNT}-deltap}{KT}$.

From equation (8), it is observed that the number of carriers in the channel reduces to zero when

$$vgs = \ln[\frac{qn_i}{C_{ox}}\ln\left(1+\gamma\frac{vds}{V_t}\right)]$$

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Where, γ is fitting parameter and n_i is intrinsic carrier concentration. Using equation (8), the total charge density in the channel is given as;

$$\text{Qcnt}= q\left(\frac{N_0}{2}\right)\cosh\left(\frac{Va}{V_t}\right)\exp\left(-\frac{V_{CNT}}{V_t}\right)[e^{beta}+\left(\frac{deltap}{KT\sqrt{2}}\right)^2\{E_i(beta)-\left(\frac{1}{beta}\right)e^{-beta}\}] \quad (9)$$

And hence finally expression for quantum capacitance in the single-wall CNTFET device is given as;

$$Cq = q\left(\frac{N_0}{V_t}\right)\sinh\left(\frac{Va}{V_t}\right)e^{-\left(\frac{V_{CNT}}{V_t}\right)}[(1+\coth\left(\frac{Va}{V_t}\right))\{e^{beta}+\left(\frac{deltap}{KT\sqrt{2}}\right)^2\left(E_i(beta)-\left(\frac{1}{beta}\right)e^{-beta}\right)- \coth\left(\frac{Va}{V_t}\right)\{e^{beta}+\left(\frac{deltap}{KT\sqrt{2}}\right)^2\left(\frac{\cosh(beta)}{2beta}-\left(\left(\frac{V_t}{beta}\right)^2e^{-beta}\right)\}] \quad (10)$$

Equation (10) shows that Cq is bias dependent [22] and proportional to the density of states (DOS). It is also observed that as Va→0, Cq reduces to zero (quantum capacitance limit). In the quantum capacitance limit, instead of holding the charge constant the gate holds the nanotube potential constant at the gate. We have also observed that for qV_{CNT}=deltap, quantum capacitance approaches toits classical limit (Cq→∞).

Now let us consider two cases;

Case1: when "beta" is negative. Equation (8) reduces to;

$$n_{CNT} \cong A\, e^{-beta} \quad (11)$$

Where, $A=\cosh\left(\frac{Va}{V_t}\right)e^{-\left(\frac{V_{CNT}}{V_t}\right)}$.

This expression predicts that the number of normalized carrier density falls exponentially for negative beta.

Case 2: When "beta" is positive. The normalized carrier density reduces to;

$$(n_{CNT})/N_0 \cong \mathrm{B} + \mathrm{C} * \mathrm{beta} \quad (12)$$

$$B = \cosh\left(\frac{Va}{V_t}\right)e^{-\left(\frac{deltap}{KT}\right)}\left[\left(\frac{3}{2}-\frac{2V_{CNT}}{V_t}\right)\right]$$

And

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$$C = (\frac{1}{2}) \cosh\left(\frac{Va}{V_t}\right) e^{-(\frac{deltap}{KT})}$$

Expression 12 shows that the number of carriers increases linearly for positive beta.

Case 3: For continuity at beta=0, it is required that A=B and hence the necessary condition for continuity is;

$$\left(\frac{vgs - Va}{V_t}\right) = (\frac{1}{2})$$

III. Simulation Results and Discussion

Following values of various parameters have been chosen for the simulation of single-wall CNTFET device; tox (oxide thickness) = 10 nm, rcnt (radius of the tube) = 1 nm, L= 10 nm, vds= 0.05 V, vgs= 0.2 V.

The lower value of drain voltage is purposely chosen so that gate has effective control of the channel over the external field. The number of carriers in the channel increases linearly with gate bias voltage due to decrease in source-channel barrier height at large gate voltage. At higher gate voltage it is observed that carrier remain insensitive towards temperature change due to access resistance limitation in CNTFET. The charge carrier density in the tube is suppressed appreciably in inversion region compared to the subthreshold region at higher drain voltage irrespective of the gate voltage.

Figures 2(a) and 2(b) respectively validate our findings that for positive beta, the normalized carrier density increases linearly whereas it falls exponentially for negative beta.

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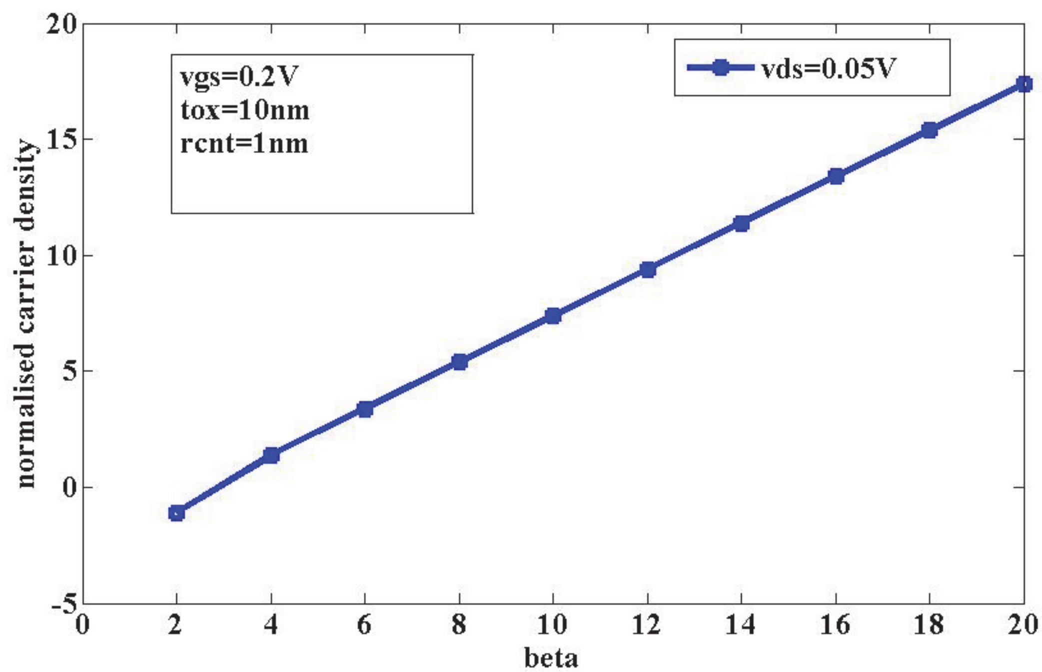

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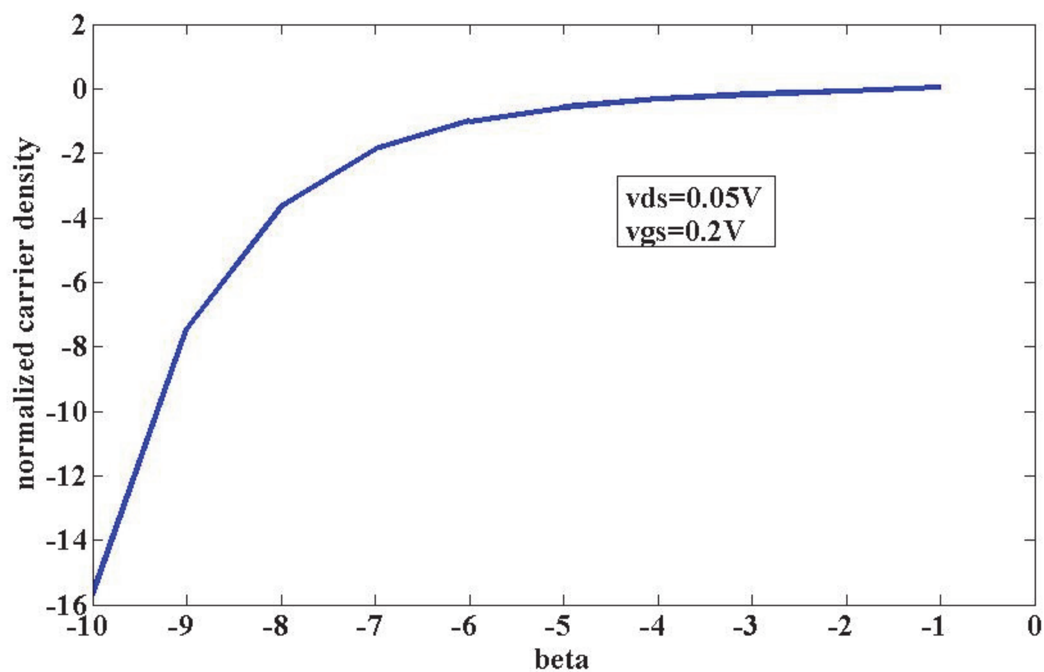

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Figure 2: Variation of normalized carrier density (a) for positive beta (b) negative beta

The developed expression (8) was validated with excellent agreement with ref. [23] models as shown in Figure 3.

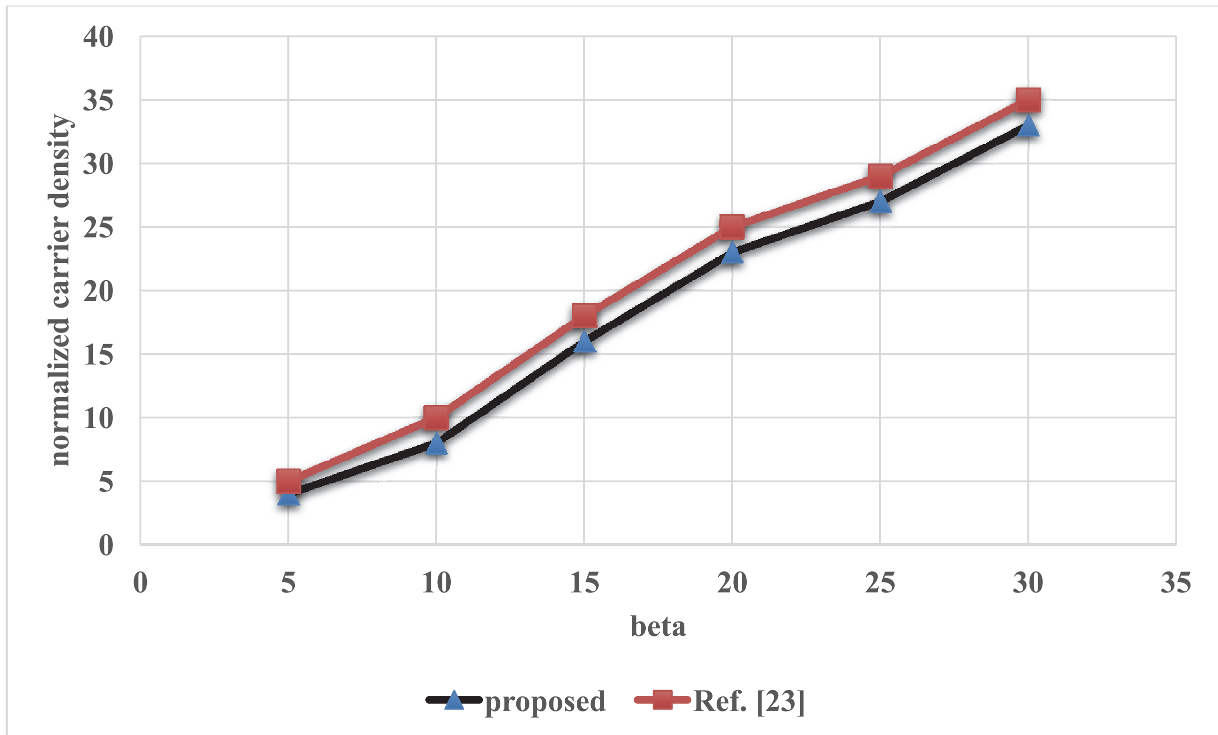

Figure 3: Comparison of normalized carrier density with equation (8) and ref. [23]

Figure 4 shows the variation of normalized log Q_{CNT} with applied voltage Va for different deltap. The charge carrier density is normalized with respect to N_0. It is observed that the number of carriers is larger in the lower sub-band compared to the higher sub-band due to lower energy required to move the carriers from the valence band to conduction band. Generally, carrier density increases with bias voltage due to increased conduction in inversion region of the device.

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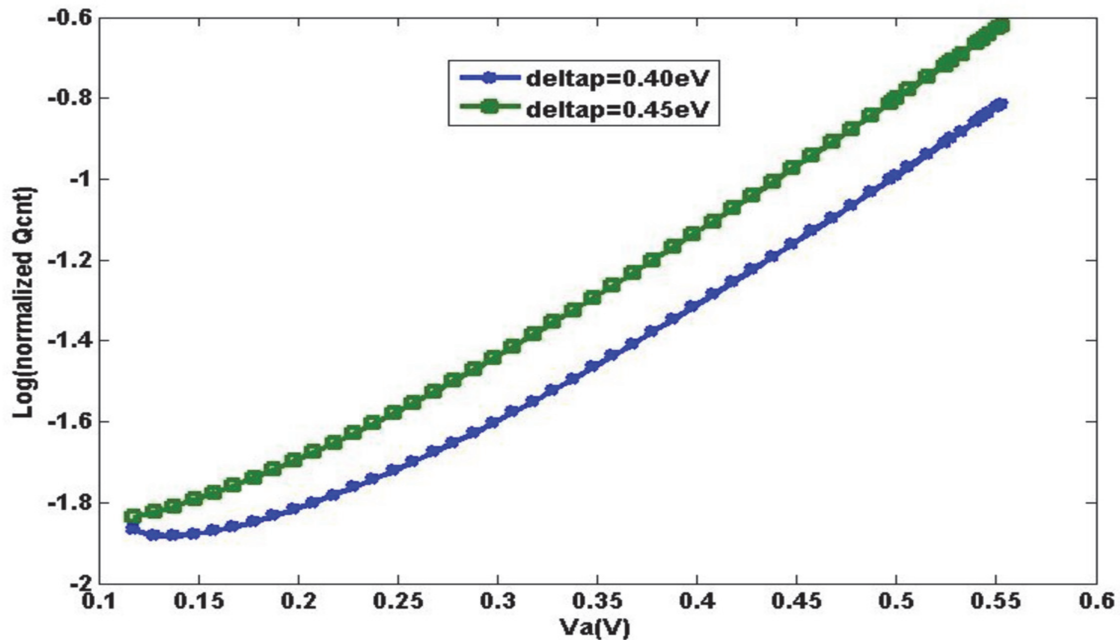

Figure 4: Variation of normalized Q_{CNT} against V_a for two sub-bands

The charge density Qcnt decreases as drain bias voltage (v_{ds}) increases because the increased drain voltage suppresses the –k half of the distribution function which reduces the charge density irrespective of sub-band value (Figure 5).

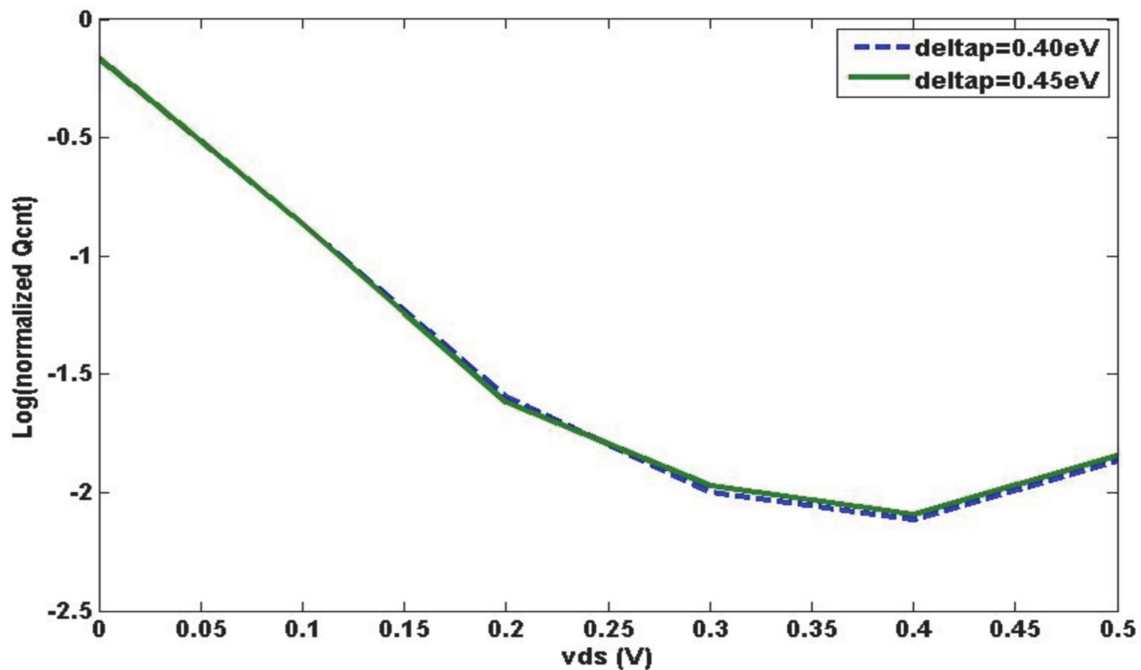

Figure 5: Normalized Q_{CNT} variation with vds for two sub-bands

Charge density Qcnt increases exponentially with gate voltage (vgs) (Figure 6) because nanotube potential is pinned by the gate voltage which results in larger charge density in the channel. An appreciable effect of deltap is observed on normalized Qcnt only at lower gate voltage due to BTBT tunneling effect.

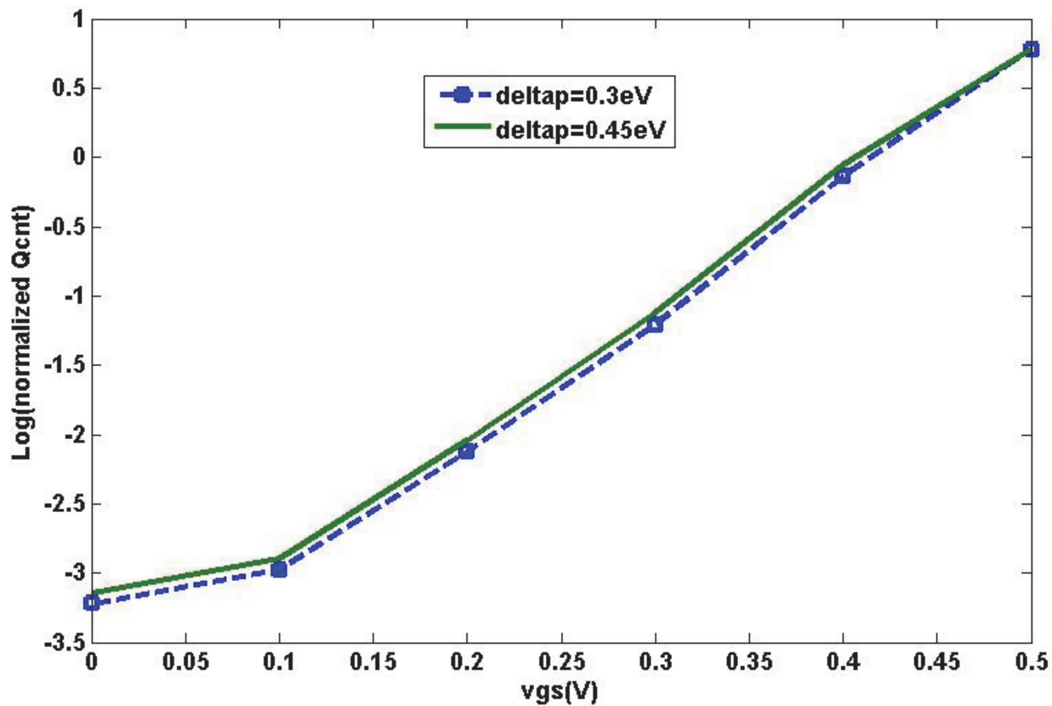

Figure 6: log (Q_{CNT}) versus vgs for two different values of deltap.

To validate the proposed analytical expression (10), we have compared the simulated results of expression (10) with the results provided in ref. [20] for tox=0.7nm. The comparison results are given in table 1. The difference between two results is due to negligence of short channel effects in the analytical expression (10).

Table 1: Comparison of quantum capacitance with ref. [20]

vds=0V, d=0.7nm, Kr=1		
vgs (V)	Quantum capacitance (F/m)	
	Calculated using	Ref. [20]

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	expression (10)	
0.0	6.32×10^{-16}	5.12×10^{-16}
0.05	4.37×10^{-15}	3.85×10^{-15}
0.10	3.02×10^{-14}	2.50×10^{-14}
0.15	2.09×10^{-13}	2.10×10^{-13}
0.20	1.44×10^{-12}	1.15×10^{-12}

The quantum capacitance measures the density of states (DOS) which undergoes a large transition as Fermi level is pushed inside the sub-bands at large gate voltage. At high voltage, upper valleys get populated which allows a continuous increase in Cq (Figure 7). Since, in CNT the energy gap is inversely proportional to the diameter of the tube, therefore, larger diameter gives lower energy gap which results in lower Cq as seen from Figure 7. The increase in quantum capacitance with increase in gate bias voltage is more pronounced in inversion region compared to subthreshold region due to dominance of quantum effect in nano-scale device.

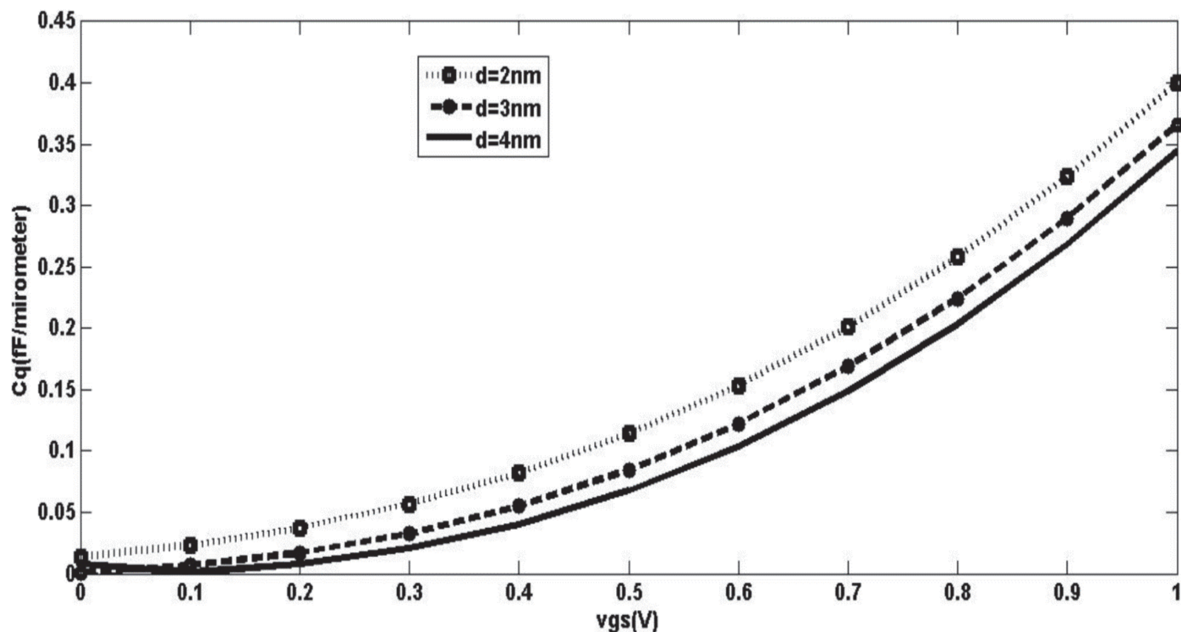

Figure 7: Variation of C_q with vgs for various tube's diameters (d)

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The energy level is smaller in the case of first occupied sub-band than the higher sub-bands. The lower energy gap of the first sub-band results in lower quantum capacitance compared to the second sub-band (deltap=0.9eV) (Figure 8).

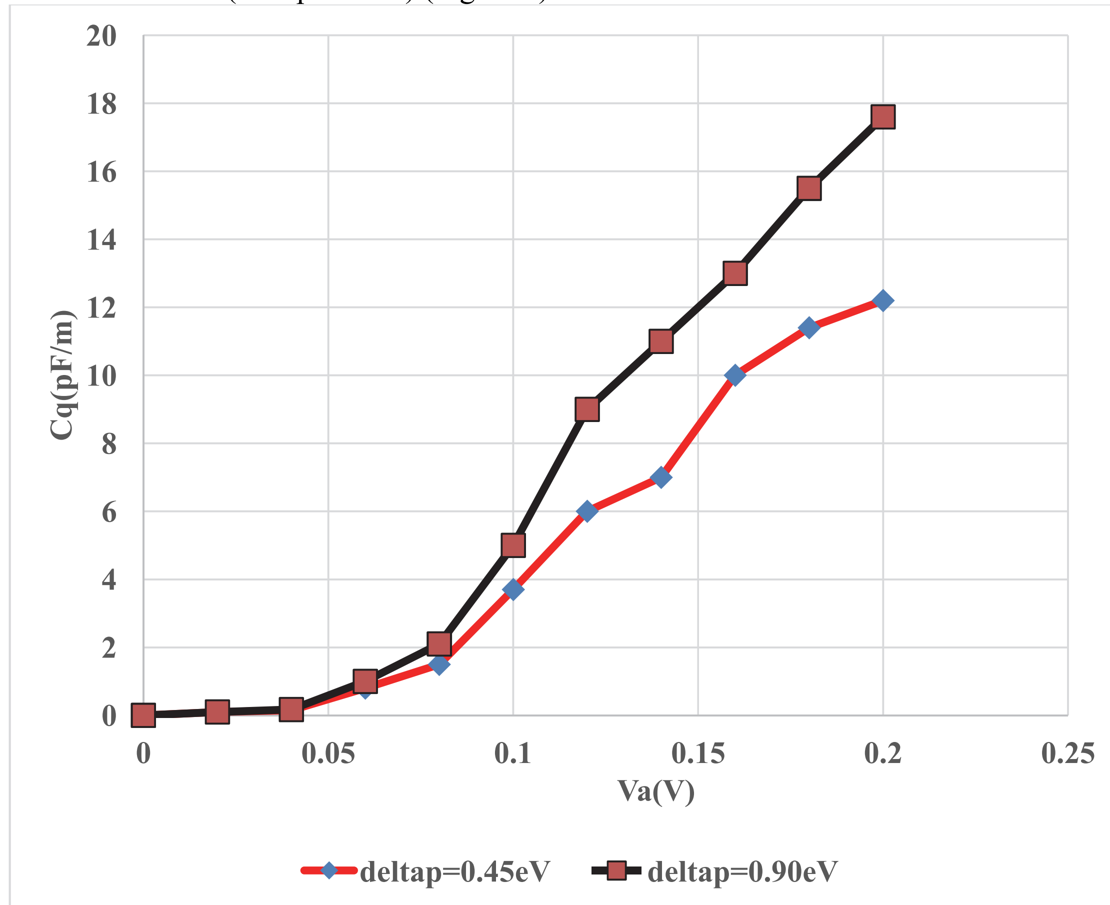

Figure 8: C_q versus V_a for first and second sub bands

At higher drain voltage, C_q takes lower value due to suppressed Fermi level in CNTFET device which results in lower density of states (DOS) as shown in Figure 9. The simulation results also suggest that by raising the drain and gate voltages, the quantum capacitance in CNTFET device can be reduced drastically.

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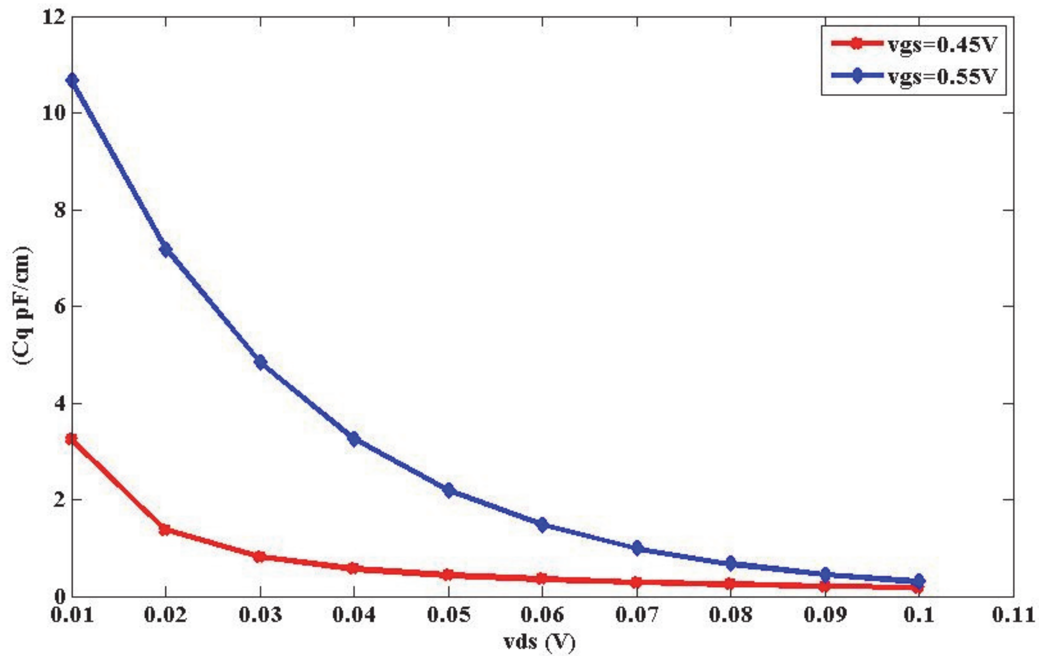

Figure 9: Variation of C_q with vds for two gate bias voltages (vgs)

In CNTFET device, high relative dielectric material (Kr) can be easily achieved which lowers the quantum capacitance due to better control of tunneling current in the channel as shown in Figure 10.

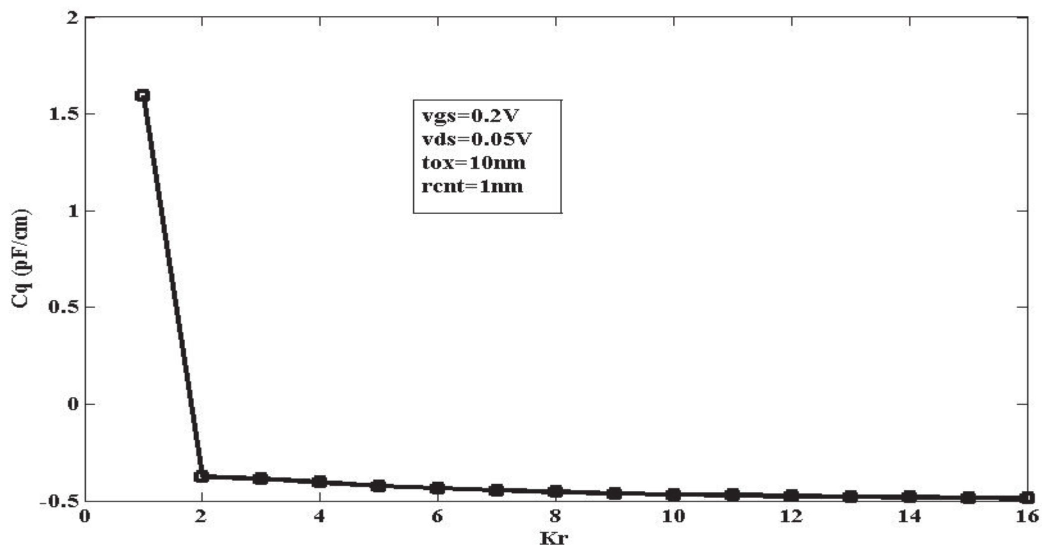

Figure 10: Effect of relative dielectric (K_r) constant on C_q

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Cq reduces for thicker gate oxide (t_{ox}) compared to the thinner oxide due to effective control of leakage current in the device irrespective of the applied gate/drain voltages (Figure 11).

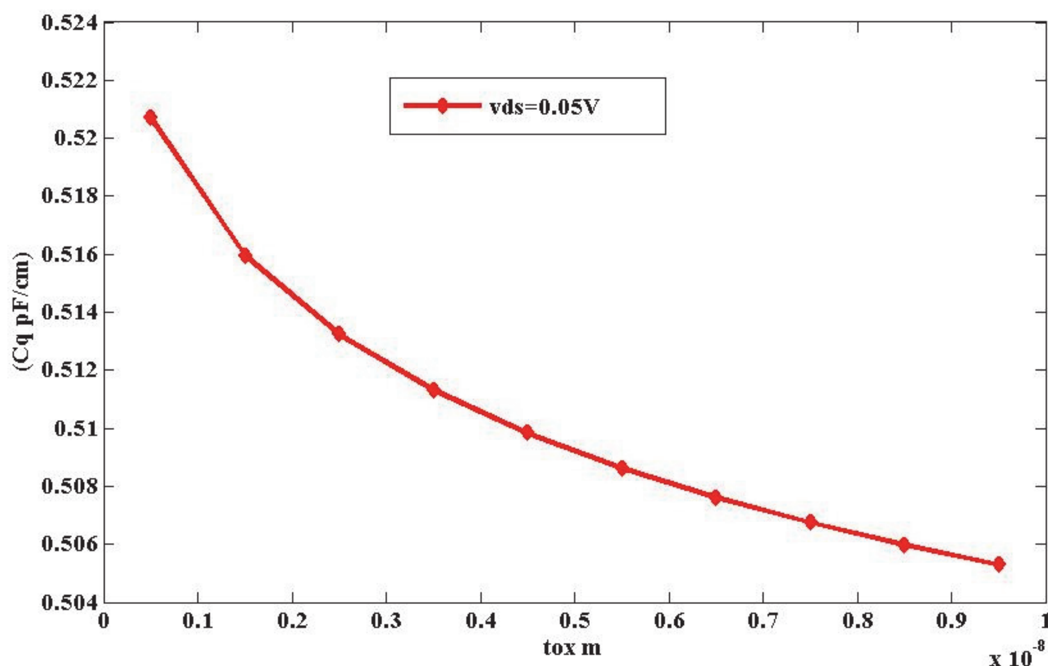

Figure 11: Effect of oxide thickness (t_{ox}) on the C_q

It is also observed that when tube of radius 1nm and gate thickness of 0.25 nm is occupied by one sub-band then quantum capacitance value approaches to approximately 4 pF/cm.

IV. Conclusion

Due to lower density of states in CNTFET devices, the quantum capacitance becomes comparable to oxide capacitance which starts to affect the gate capacitance. In this paper an analytical expression for the quantum capacitance has been proposed. In subthreshold region, due to negligible quantization effect quantum capacitance does not affect the performance of CNTFET device severely compared to the inversion region. In general, quantum capacitance takes lower value for larger oxide thickness and relative permittivity of the gate material. Quantum capacitance also suppressed at higher drain voltage and larger tube's diameter. Lower quantum capacitance results in improved propagation delay and reduced leakage current which improves the performance of the device.

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