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Two Low Power and High Efficient Full Adder Cells Based on CNTFET Technology

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*Abstract-*This paper presents two novel full adder cells based on Carbon Nanotube Field Effect Transistor (CNTFET) technology. According to unique specifications of CNTFET, and its similarity to conventional MOSFET technology, CNTFET technology is considered as a good successor for conventional MOSFET technology in nano-electronic in near future. The full adder cells benefit from less power consumption, delay time and occupied area comparing to peer designs. All CNTFET presented and previous designs have been carried out using Synopsys HSPICE in a realistic test bench and other various strict conditions in 32 nm technology. The Simulation results show that presented adders perform better comparing the previous designs.

1. Introduction

Full adder is among the greatest useful logic blocks, it is considered as the key arithmetical component of all digital systems [1]. Several operations like multiplying, subtraction, division and arithmetic operators are done by means of addition [2]. In a nutshell, the full adder cell and its output signals exclusively are among the most practical logic blocks in VLSI circuits. The critical path of almost all digital systems includes full adder blocks [1].in case being improving the adder cell performance can improve the whole system

 consequently

Complementary Metal Oxide Semiconductor processors (CMOS) have been dominant technology for many decades. Nowadays many applications such as telecommunications, transportation, education and medical care are dependent on the technology (CMOS) [3]. Meanwhile

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the needs of scaling down the size of transistors brought many challenges and difficulties for circuit designers. Some of these challenges include very high leakage currents, decreasing the gate control, high power density, large parametric variations, and high lithography costs [4].

To overcome of these problems, some technologies have been presented previouslylike: Carbon Nanotube Field Effect Transistor (CNTFET), SingleElectron Transistor (SET), GrapheneNanoribbon Transistor (GNRT), and Quantum Carbon Automata (QCA) [5, 6, and 7].

However, CNTFET technology because of its unique characteristics such as Ballistic transport ability which brings about high-speed operation, same mobility for both nCNTFET and pCNTFET types which directs to simple transistor sizing process, and the ability of adjusting desired threshold voltage by adopting proper diameter for the nanotubes(Eq.1, 2), are definitely worth to discussion[7].
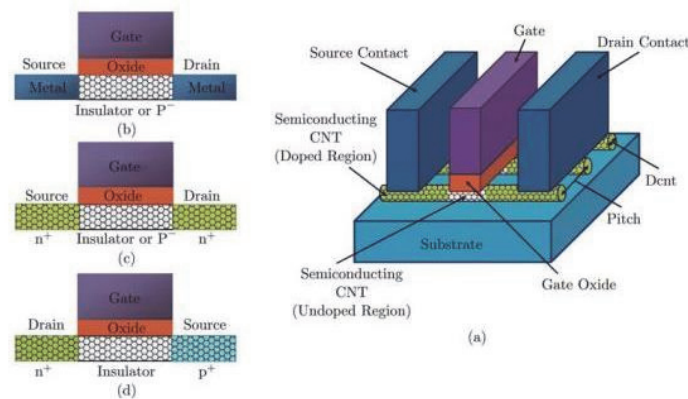

Figure 1: (a) A typical CNTFET device; Different types of CNTFET device (b) SB-CNTFET (c) MOSFET-like CNTFET(d)   T-CNTFET [7].

$$D_{CNT} \approx 0.0783 \times \sqrt{n_1^2 + n_2^2 + n_1 n_2} \qquad \text{(Eq.1)}$$

$$V_t \simeq \frac{E_g}{2e} = \frac{\sqrt{3}}{3} \frac{\alpha E_\pi}{e D_{CNT}} \simeq \frac{0.43}{D_{CNT}} \qquad \text{(Eq.2)}$$

In this paper, two novel 1-bit high-speed and high-efficient full adder cells are presented. The proposed designs are based on pass transistor logic. The Sum and Cout signals are generated separately.

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The key target is to achieve high performance and high efficiency while the proposed design has the advantage of full voltage swing outputs, high driving power, robustness and the ability of employed in high frequencies and low voltages. Different conventional full adder cells with the same logic style have been selected for evaluation. High speed, low power consumption, and novelty are the main issues which make the presented designs an ideal selection. All circuits are simulated with HSPICE and 32 nm CNTFET technology in a realistic environment and other various conditions. The simulation results reveal the superiority of the proposed design.

The rest of the paper is prepared as follows: In Section 2, previous researches are reviewed. Proposed design will be presented in Section 3. Section 4 contains simulation results. Finally, Section 5 covers conclusion.

2. Previous Research

Figure 2 demonstrated a 23 T full adder cell [8]. The design is a combination of transmission gate and pass-transistor logic. The inverted outputs are first generated. Formerly, two inverters are utilized for final conversion. In spite of adding extra transistors and increasing longer critical path, it brings about higher speed and driving capability in case of existing high number of fan-outs. The intermediate XOR and XNOR functions are not generated in a parallel manner which leads to longer critical path within the cell. A multiplexer-based structure is used to generate the other output signal (C_{out}) [1].
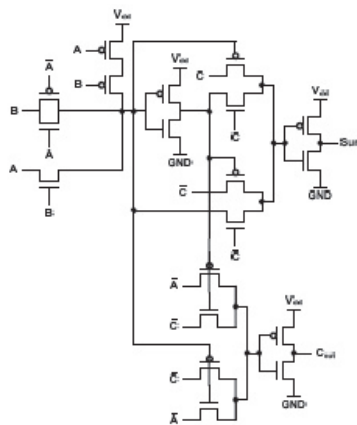

Figure 2: 23T Full Adder Cell Presented in [8].

Figure 3 shows a hybrid full adder cell [9]. Two different circuits are used to generate output signals simultaneously. The Sum output is generated by means of two different cascaded XOR/XNOR cells. The first cell is a pseudo-DCVS circuit which generates both functions using only 6 transistors. The following one is a high speed DCVS circuit. It can produce both sum and sumnot. However, an inverted

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input is required for the 2nd stage, albeit the cell arrangement eliminates using extra inverter. Hence, complementary inputs are not essential within the whole cell. Though, long critical path together and a low driving capability of the DCVS structure leads to low speed. The last inverters are added to decrease the delay particularly while driving high load capacitors. To generate the C_{out} the bridge style architecture is employed [9].
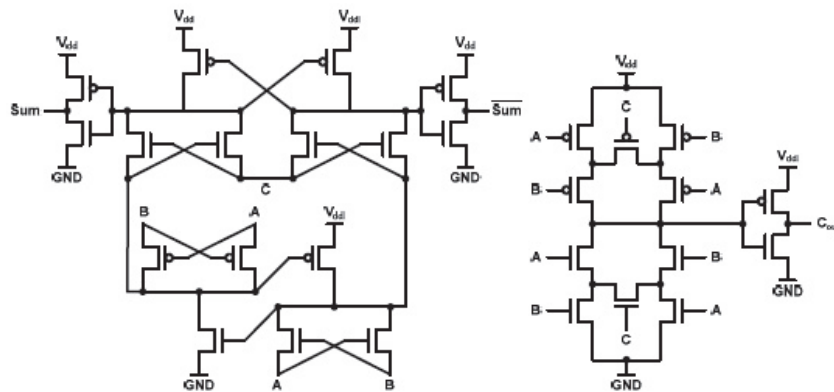

Figure 3: Hybrid Full Adder Cell Presented in [9].

The CNT-CPL designed discussed in figure 4 creates an adder block uniquely [10]. Its critical path includes only two pass transistors. In addition, designing based on CNTFET technology brings higher speed, and can overcoming the drawback of non-full-swing nodes [10]. However, low driving capability is the main disadvantage of the cell because of the applied pass-transistor logic. Although it is possible to implement the inverted outputs and use inverters to obtain higher driving power, however its lead to higher transistor count [10]. In addition, cascading blocks in serial manner causes signal distortion especially in high frequencies. Finally, the same structures are used for both Sum and C_{out} [1].
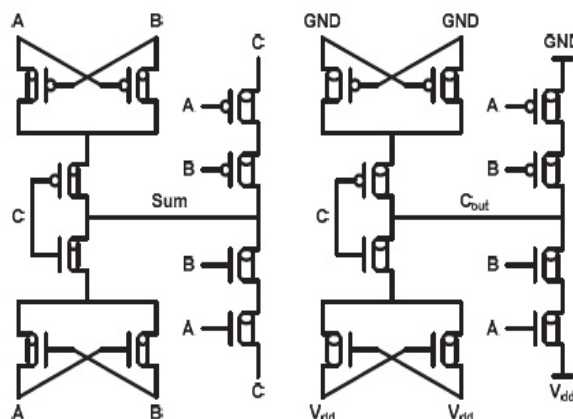
Figure 4: CNT-CPL Full Adder Cell Presented in [10].

The last investigated full adder cell is another CNTFET-based circuit represented CNTFA (Fig. 5) [11]. This is also based on intermediate XOR and XNOR functions and pass-transistor logic. The generated XOR/XNOR outputs are employed as selectors in a multiplexer-based structure at the 2nd stage to generate Sum.

Another pass-transistor based block at the 2nd stage is utilized to generate the C_{OUT} in parallel with Sum. The designs benefit from full-swing operation, low power consumption and high-speed computation. However, it suffers from low driving capability [1].
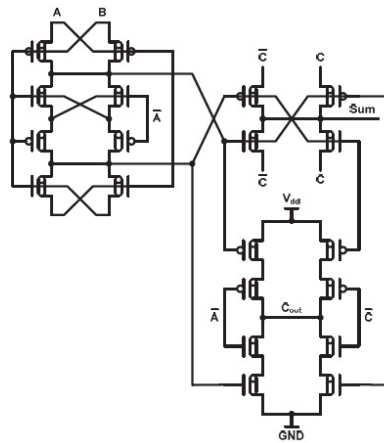

Figure 5: CNTFA Cell Presented in [11].

3. PROPOSED FULL ADDER CELL

Figure 6 shows the 1st presented design includes 19 transistors. In this design the elimination of using the invetred values of both input (ANOT, BNOT) signals lead to less number of transistor and less occupied area. One XOR unit is employed to omit the use of the inverters. So, the critical path of the design has decreased. This can improve the delay time and also the power delay product (PDP).
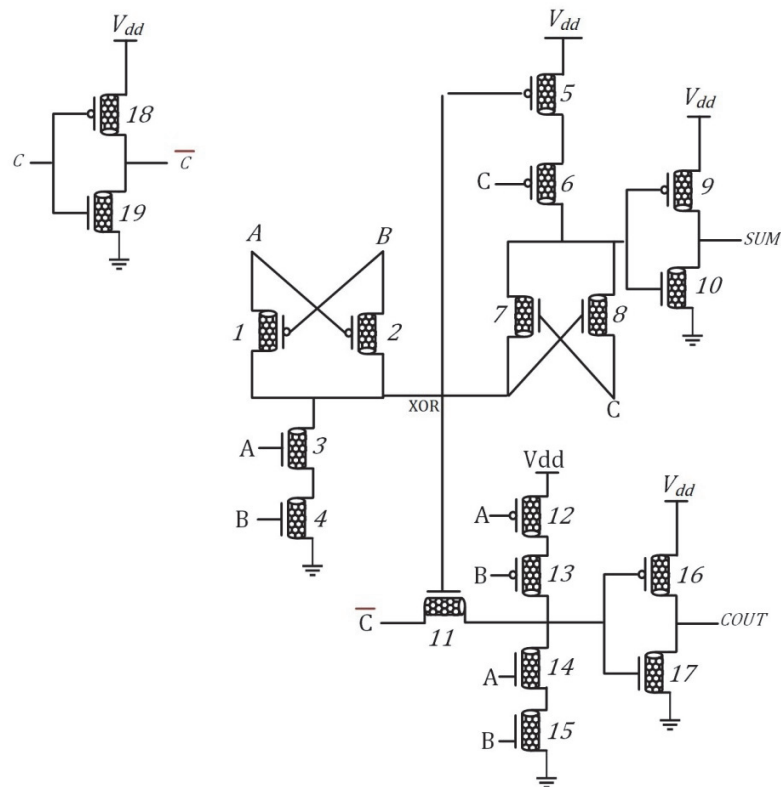
Figure 6: Full Adder Circuit with 19 Transistors (19T proposed).

The 2nd presented full adder cell includes 12 transistors (Fig.7). The design is a combination of transmission gate and pass-transistor logic. Less number of transistors is significant point of the design. This achievementleads to decrease the power consumption. The design also benefit from symmetrical manner that leads to ease of transistor sizing.
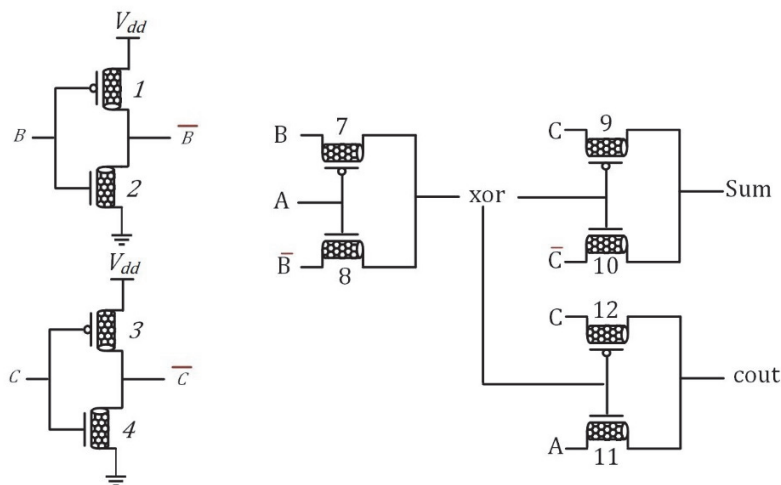
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Figure 7: Full Adder Circuit with 12 Transistors (12T proposed).

4. SIMULATION RESULTS

All of the four conventional and presented designs, in Section 2, have been selected for comparison.

The choice of each circuit is based on its features such as high speed, low power, novelty, and structural similarity to the presented designs. The proposed design and the other full adder cells have been simulated with Synopsys HSPICE and 32 nm CNTFET technology [11]. Input Buffers together with a 2fF load capacitor have been applied to make a practical condition for all presented and previous designs. Transistor sizing details for both proposed designs are shown in table 1 and 2.

Table 1. CNT circuit proposed with 19 Transistors.

Transistors	DCNT(nm)	#CNTs
1,2	2.7405	10
3,4	2.2707	3
5,6	1.4877	3
7,8	2.7405	5
9,10	1.4877	16
18,19	1.4877	5

Table 2. CNT circuit proposed with 12 Transistors.

Transistors	DCNT(nm)	#CNTs
1 to 4	1.4877	5
7 and 8	4.5414	4
9	3.8367	3
10	3.6018	4

11 and 12	2.7405	3
13 and 14	1.8009	9

The simulation results are shown in Table 3. The simulation has been carried out at 0.7V power supply with 100MHz operating frequency at room temperature.

Table 3. Simulation results all circuits at room temprature and 0.7 supply voltage and 100 MHz operating frequency.

Type	PDP(aJ)	Power(μW)	Delay(psec)
19T proposed	3.3479	0.19186	17.45
12T proposed	4.2895	0.19812	21.651

The complete input pattern [1] with 56 transitions has been fed to measure the delay of each cell.

In order to show the worst delay, all possible transitions in this input pattern have been checked [11]. The delay parameter has been considered from the time that the input signal reaches V_{dd} to the time that the output signal touches the same voltage level. The maximum delay of all transitions is considered as a cell delay. The average power consumption during all transitions is called as the power consumption parameter. Finally, the PDP, which creates a balance between delay and power, is calculated.

$$PDP= delay * power \qquad (Eq.4)$$

The proposed full adder cells show better performance comparing peer designs. The simulation has been carried out at 0.9 V, 0.8 V, and 0.7 V power supplies with 100 MHz operating frequency at room temperature (Table 4).

Table 4. simulation results at room temprature and 100 MHz operating frequency versus different supply voltages. .

Vdd	0.7 V	0.8 V	0.9 V

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Delay(psec)			
23T Full Adder cell [8]	205.23	145.79	115.4
Hybrid Full Adder [9]	252.58	142.42	113.58
CNT-CPL Full Adder Cell [10]	33.854	30.267	27.376
CNTFA Cell [11]	35.486	28.872	25.393
19T proposed	21.112	17.45	16.203
12T proposed	25.517	21.651	18.787
Power (μW)			
23T Full Adder cell [8]	0.2219	0.3122	0.4459
Hybrid Full Adder [9]	0.2633	0.3683	0.5403
CNT-CPL Full Adder Cell [10]	0.2326	0.3138	0.6512
CNTFA Cell [11]	0.1518	0.2011	0.2630
19T proposed	0.16019	0.19186	0.25769
12T proposed	0.15627	0.19812	0.24879
PDP (aJ)			
23T Full Adder cell [8]	45.542	45.574	51.457
Hybrid Full Adder [9]	66.494	52.456	61.374
CNT-CPL Full Adder Cell [10]	7.8739	9.4986	17.828
CNTFA Cell [11]	5.3679	5.8057	6.6792
19T proposed	3.382	3.3479	4.1755
12T proposed	3.9875	4.2895	4.674

The proposed cells have the less delay among the compared adders presented in Table 4. For instance, 12T and 19T designs are 25.01% and 28.26% faster than The CNTFA Cell which is the fastest cell among the adders.

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Another characteristic of driving capability is the ability of working in larger circuits. So, three cascaded cells have been studied as the second simulation setup (Fig. 8). The Sum signal in the 1st possible cascading test-bed (Fig. 8(a)), the Sum is considered as both the first and the second inputs of the following cell, however the Cout signal is the 3rd one. Concerning Eq. 4 and Eq. 5, the duplication of Sum leads to a swap in the wave forms of former output signals.
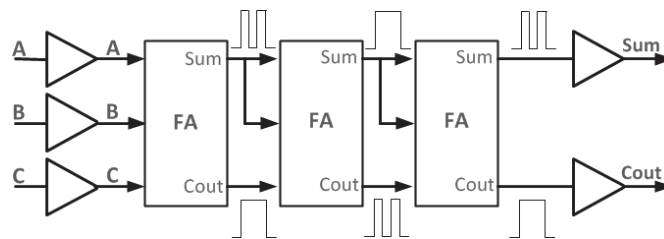
It worth to mention, there is not a swap in the waveforms by applying the 2nd cascading simulation setup (Fig. 8(b)) as the C_{out} signal is repeated, (Eq. 6 and Eq. 7). Hence, an even number of cascaded cells is also possible to be comprehended.

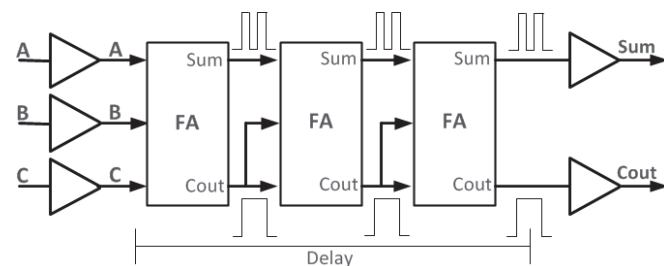$$\text{Sum (Next Cell)} = \text{Sum} \oplus \text{Sum} \oplus \text{Cout} = \text{Cout} \tag{1}$$

$$\text{Cout (Next Cell)} = \text{Majority (Sum, Sum, Cout)} = \text{Sum} \tag{2}$$

$$\text{Sum (Next Cell)} = \text{Sum} \oplus \text{Cout} \oplus \text{Cout} = \text{Sum} \tag{3}$$

$$\text{Cout (Next Cell)} = \text{Majority (Sum, Cout, Cout)} = \text{Cout} \tag{4}$$

(a)

(b)

Figure 8. Cascading Simulation setups [10].

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Input and output buffers are also in employment to make even more severe conditions. The output wave forms of the third cell are shown in Fig. 9 for the proposed designs.
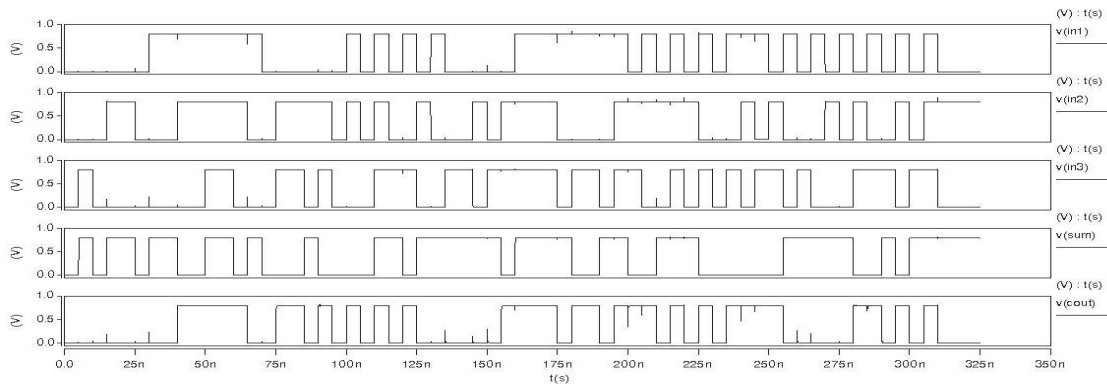

Figure 9. Output wave forms of the third cell for the proposed design.

Finally, Monte Carlo transient analysis with a number of 30 iterations for each simulation is analysed to examine sensitivity to process variation. A standard deviation in the range of 0.04 nm to 0.2 nm is measured for each diameter value [11]. The proposed designs work reliably in case of procees variation (Fig.10).
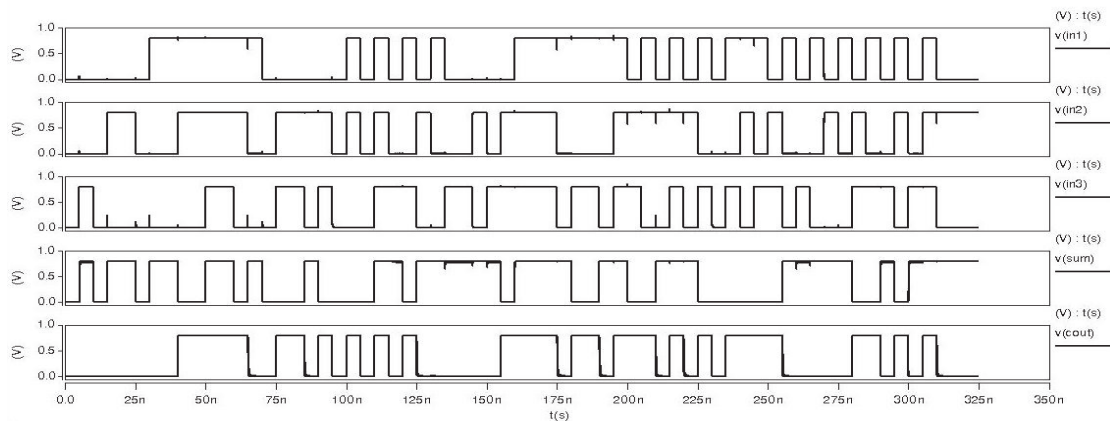

Figure 10. Output wave forms of Monte Carlo transient analysis.

To examine the immunity of the propsed designs to the ambient temperature noise and variations, all designs have also been simulated in a vast range of temperatures from 0^{oC} to 70^{oC}.

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The results are presented in Fig.11. In spite of temperature variation, the results show that the proposed designs have normal functionality. They also beat other designs in terms Of performance.
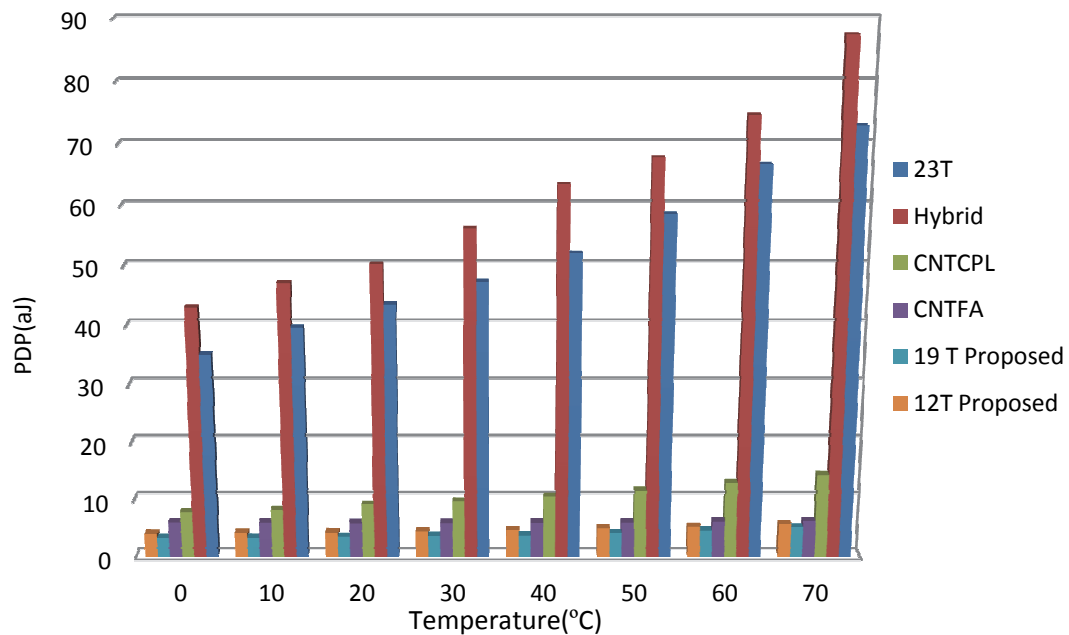

Figure 11. PDP versus Temperature Variations.

Today, the capability of working in high frequencies in VLSI circuits is necessitated. In case being, all circuits are simulated at higher frequencies such as 500 MHz and 5 GHz. Figure 12 displays the cells performance versus frequency increments. It can be understood that the proposed structures have the best performance comparing other circuits at high frequency operation.
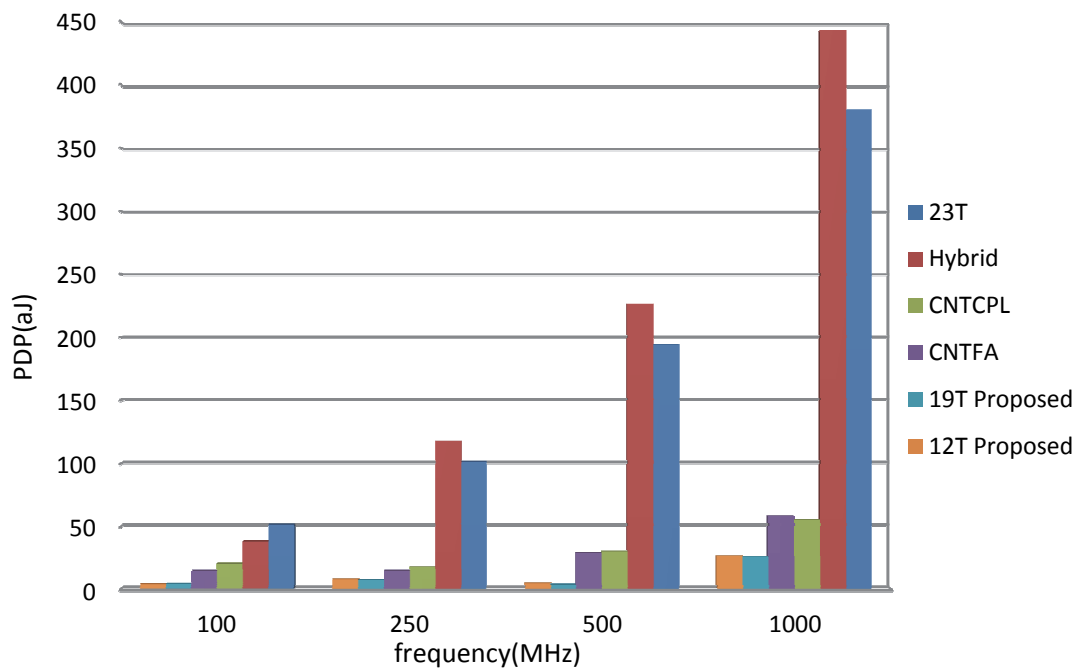
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Figure 12. PDP versus Different Operating Frequencies.

To study the driving power of the proposed designs precisely, different capacitors are used as the output load. The capacity of output load is changed from 2 fF to 20 fF. Cell delay versus different output loads is shown in Fig.13.
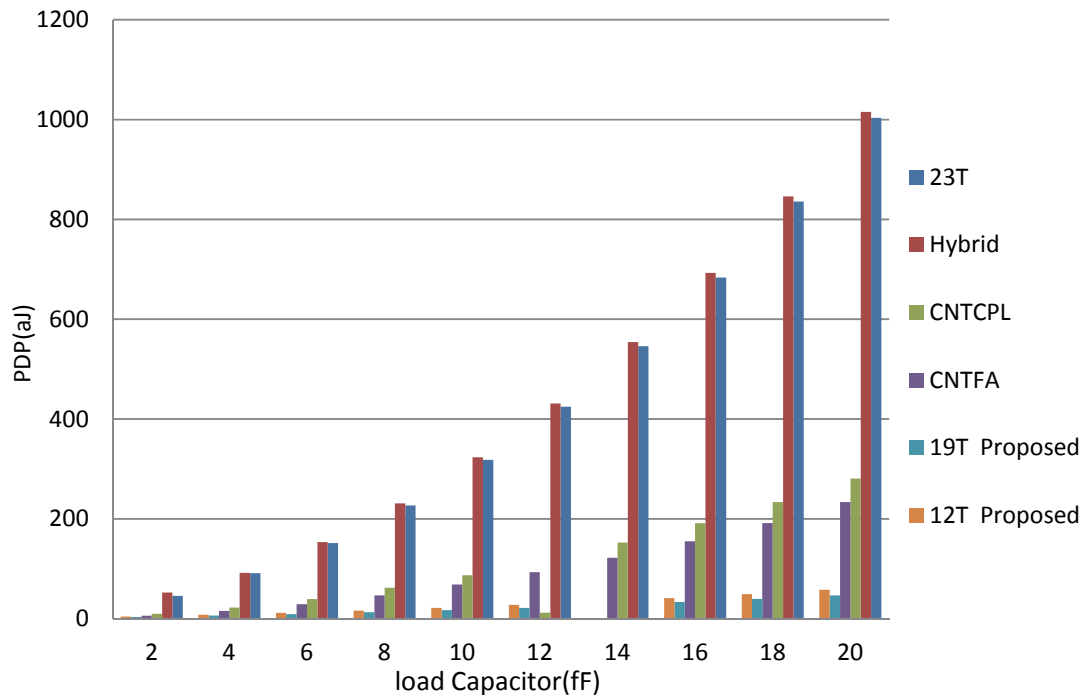
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Figure 13. PDP versus Load Variations.

5. Conclusion:

In this paper, two full adder cells based on CNTFET technology have been presented. The 1st design employs 19 transistors and the 2nd design uses 12 transistors. The designs benefit from less number of transistor, which leads to power and PDP decrease in addition to less area comparing previous designs.

The proposed full adders operates about 26.1% faster with also 4.62% less power than the next best adder block in a practical condition regard to simulation results.

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برای تغییرات لازم در شکلهای11و12و13 خود چارت رو از اکسل بیارید

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