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SOI based nanowire single-electron transistors: design, simulation and process development

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Abstract

One of the great problems in current large-scale integrated circuits is increasing power dissipation in a small silicon chip. Single-electron transistors which operate by means of one-by-one electron transfer, is relatively small and consume very low power and suitable for achieving higher levels of integration. In this research, the four masks step are involved namely source and drain mask, Polysilicon gate mask, contact mask, and metal mask. The masks were designed using ELPHY Quantum GDS II Editor with a nanowire length and nanowire width of approximately 0.10μm and 0.010 μm respectively. In addition, the process flow development of SET and the process and device simulation of SET are also explained in this paper. The Synopsys TCAD simulation tools are utilized for process and device simulation. The results from the device simulation showed that the final SET was operating at room temperature (300K) with a capacitance estimated around 0.4297 aF.

1. Introduction

Single-electron transistor (SET) is a key element in single electronics where device operation is based on one-by-one electron manipulation utilizing the Coulomb blockade effect. The SET are often discussed as elements of nanometer scale electronic circuits because SET can be made very small and can detect the motion of individual electrons. However, SET has low voltage gain, high input impedances, and is sensitive to random background charges [1]. This makes it unlikely that SET would ever replace field-effect transistors in applications where large voltage gain or low output impedance is necessary.

SETs can potentially take the industry all the way to the theoretical limit of electrons for computing applications by allowing the use of a single electron to represent a logic state [2]. The first application for SET could be for the memory and special applications in metrology, such as primary thermometers and supersensitive electrometers [2].

In this paper, we focused on the SET mask design, process flow development, and process and device simulation. An introduction of the single-electron transistor is described in the next section. The mask design will be explained in the section 3. Section 4 and section 5 will discuss the process flow development and the process and device simulation, respectively prior to conclusions.

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2. Single-Electron Transistor (SET)

The most fundamental three-terminal single-electron device is called single-electron transistor [3-5]. SET is always three-terminal devices with gate, source, and drain, unlike quantum dots and resonant tunneling devices which may be two terminal devices without gates [6]. The SET is expected to be a key device for future extremely large-scale integrated circuits because of its ultra-low power consumption and small size. The schematic structure of SET is shown in Figure 1.

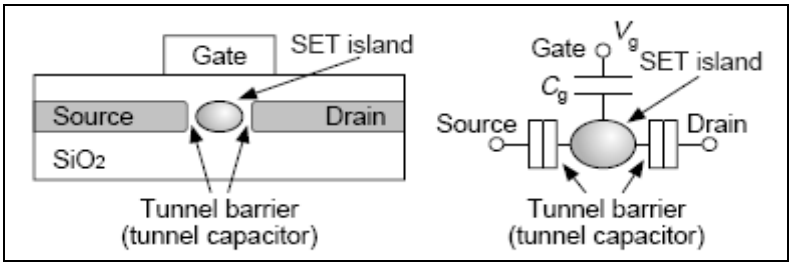

Fig. 1: Schematic structure and equivalent circuit of a single-electron transistor (SET) [7].

As shown in the Figure 1, the device must have a small island together with a gate electrode coupled to the island with gate capacitance, C_g. Source and drain electrodes are attached to the island via a tunnel barrier. In addition, SET is a device whose operation relies on single electron tunneling through a nanoscale junction. The operation principle of SET is show in Figure 2.

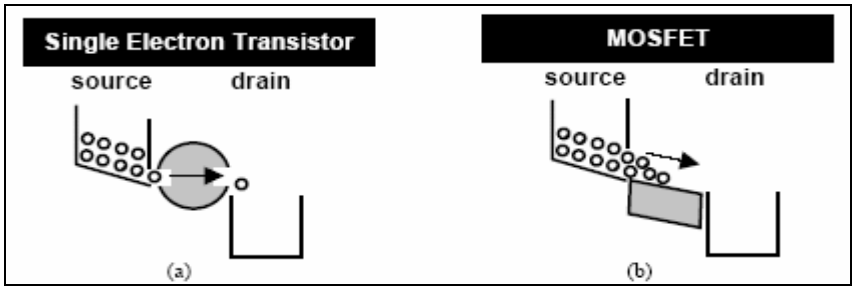

Fig. 2: Transfer of electrons is (a) one-by-one in Single Electron Transistor, which is in contrast with (b) conventional MOSFET where many electrons simultaneously participate to the drain current [8-9].

From Figure 2.4, many electrons (1000-10, 000 electrons) [10] simultaneously participate from the source to the drain current in the conventional MOSFETs. On the contrary, the electrons in SET devices are transferred one-by-one through the channel, consume very low power and small size [11]. These features are suitable for achieving higher levels of integration. In addition, SET has unique features that conventional MOS transistors do not have. The first one is SET can have many gates (gate and back gate) [11]. The other one is oscillatory conductance as a function of a gate voltage [12]. Therefore, it is generally assumed that single-electron devices have potential to be much faster than conventional MOSFETs.

3. Set Mask Design

The SET masks are designed using ELPHY Quantum GDS II Editor Software. In this study, SET masks comprises a source and drain mask, a gate mask, a contact mask, and metallization mask. The SET mask designed is started with source and drain mask as shown in Figure 3.

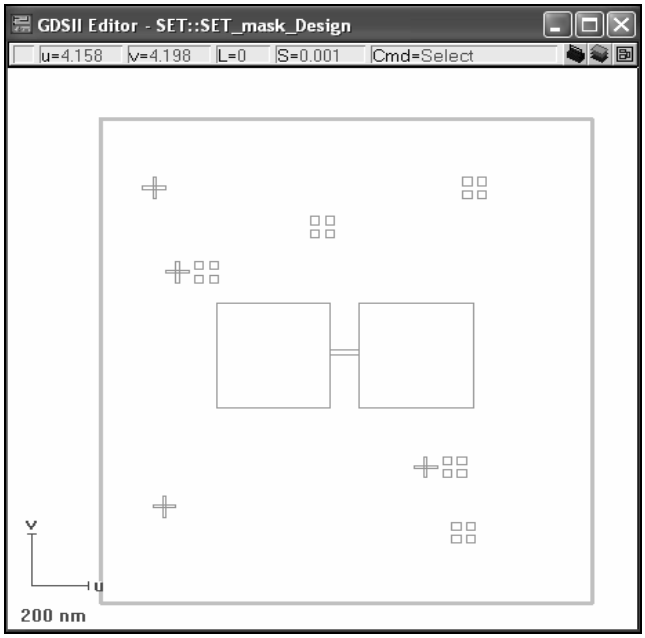

Fig. 3: The source and drain mask.

From Figure 3, the source and drain mask is used to control the heavily phosphorous doped and create the source and drain region of the transistor [13]. The source and drain region is designed with the width and length of 400 nm. This dimension was chosen based on the previous research have been reported [14, 15-16].

The spacing between the source and drain region is called a channel [17] or nanowire [18]. The width of the nanowire is 10 nm and the length is 100 nm. The nanowire is used to define the gate region. In this research, we designed the nanowire with such dimension because we want the device work at room temperature operation [15-16, 19]. Besides, the total capacitance of SET can be reduced to a value of the order of 1 aF [14-16] since the size of the silicon island become as small as around 10 nm.

The second mask is polysilicon gate mask. As shown in Figure 4, the mask is used to deposit polysilicon on the wafer. The width of the gate is 500 nm and the length is 100 nm. After the unwanted polysilicon areas are removed, the polysilicon gates over the gate oxide is defined using this mask. The polysilicon gates have a higher resistance than aluminum (Al) gates [20-21].

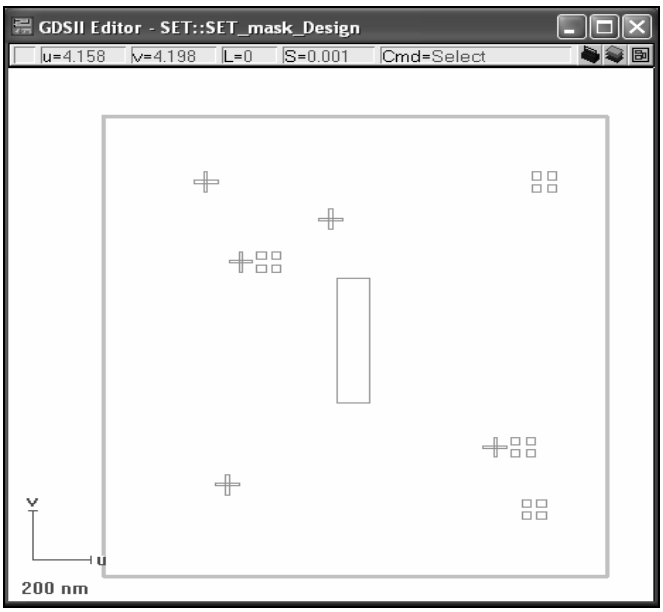

Fig. 4: Polysilicon gate mask.

The third mask is contact mask (see Figure 5). The width and length of the contact is 200 nm by 200 nm. This mask is used to define an opening to the source and drain so the metal lines in metallization process are connected to the source and drain. The etching process opens the contact holes. The polysilicon gate serves as a mask to allow precise alignment of the source and drain [18].

Finally, the interconnection was done by using metallization mask (Figure 6) for electrical characteristic. The width of the metal is 200 nm and the length is 500 nm. The uncovered aluminum film on the wafer will be etched away by using metallization mask.

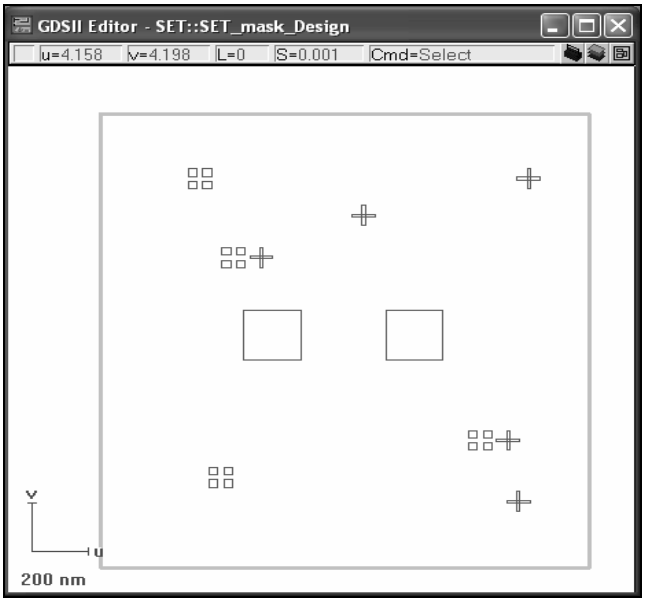

Fig. 5: Contact mask.

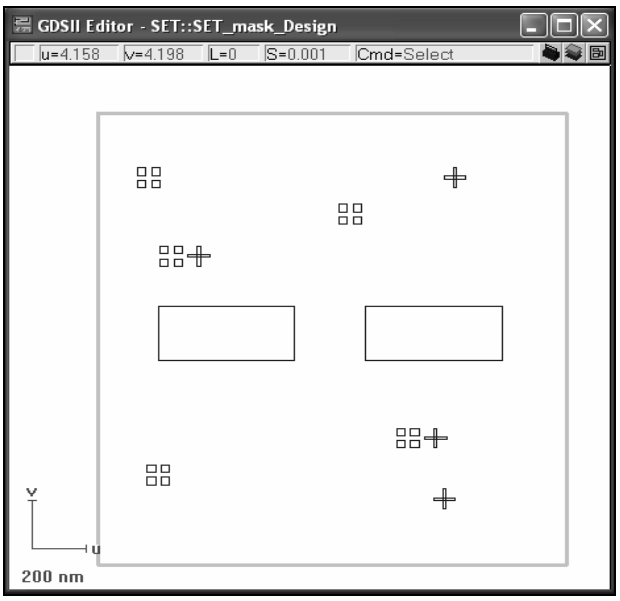

Fig. 6: Metallization mask.

In principle, the layout of the masks is shown in Figure 7. This figure clearly shows a complete SET device, which consists of a source and drain region, poly-silicon gate, a contact window, and metallization area. The cross-section of the device will determine which region that should be masked.

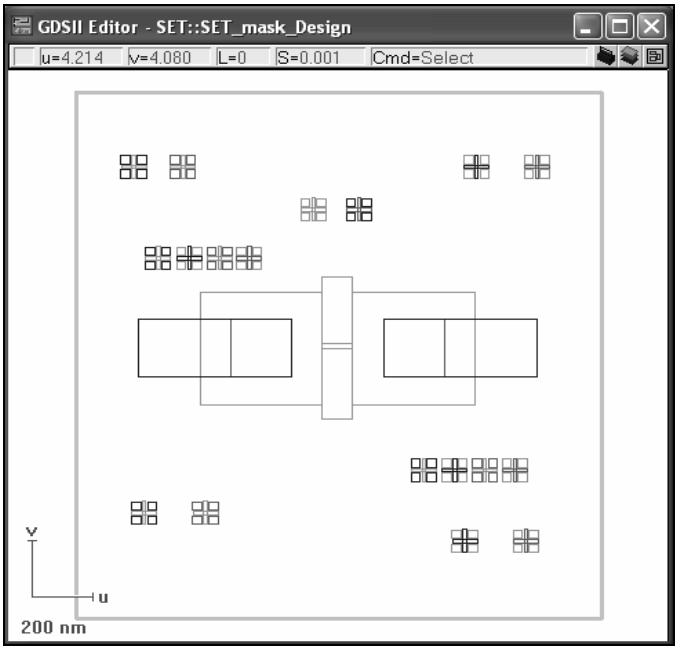

Fig. 7: Mask layout designed using ELPHY Quantum GDS II Editor Offline Software.

4. Process flow development for SET fabrication

The most difficult issue in fabricating SET is the island size of SET. For SET operation at finite temperature T, the island should be small to maintain the Coulomb blockade condition which is the charging energy, E_C of the island [22] is

$$E_C = e^2/2C_\Sigma >> k_B T \quad (1)$$

where C_Σ is the total capacitance of the SET island, k_B is Boltzmann's constant and T is the temperature of the system. It is necessary that the SET island has to be smaller than 10nm for the operation at room temperature.

In order to fabricate SET, e-beam lithography combined with an image reversal process using inductive coupled plasma (ICP) etcher will be used. E-beam lithography has the ability to fabricate patterns having nanometer feature sizes because of its very short wavelength and reasonable energy density characteristics. The main advantages of e-beam lithography over the conventional lithography techniques include very high resolution and versatile pattern formation [23].

In principle, this fabrication consists of four major processes which are source/drain and nanowire formation, polysilicon gate formation, contact formation, and metallization. The device characteristic will be measured by a precision semiconductor parameter analyzer which is located in the Failure Analysis Laboratory. In addition, scanning ion mass (SIM), scanning tunneling microscope (STM), tunneling electron microscope (TEM), scanning electron microscope (SEM) and other characterization tools will be utilized as well to characterize the device. The ten processing steps of SET process flow that involve changes to the surface of the wafer are shown in Figure 8.

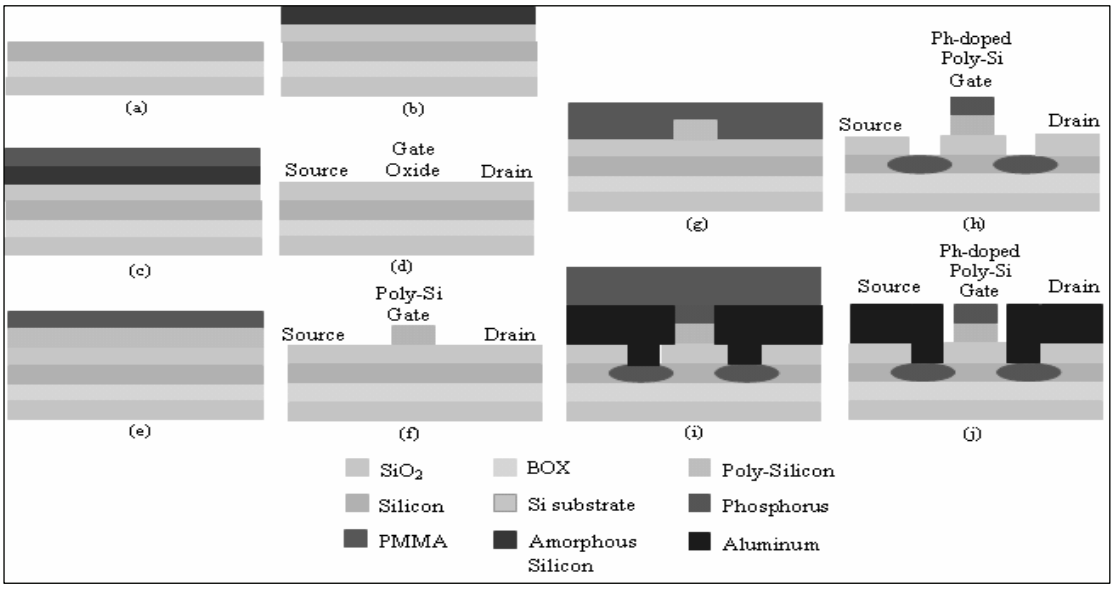

Fig. 8: The cross-section illustrating each step of the process. (See text for details.)

The SET under study is fabricated on p-type silicon-on-insulator (SOI) wafers <100> with the resistivities of 1-20 Ωm. The fabrication of SET started with cleaning the SOI wafer (Figure 8(a)) with acetone and HF to remove both organic contaminants and the native silicon dioxide from the surface. The wafer is rinsed with deionized (DI) water and spun dry. The sheet resistance of the wafer is measured to provide comparative data for calculations. Then, a 30 nm thick silicon oxide (SiO_2) and 40 nm thick amorphous silicon were sequentially deposited on the wafer surface (Figure 8(b)) using Physical Enhanced Chemical Vapor Deposition (PECVD).

A 50 nm thick Polymethyl methacrylate (PMMA) resist is subsequently coated on the amorphous silicon layer for pattern creation (Figure 8(c)). The first mask (Figure 3) is transferred onto the PMMA layer using the e-beam lithography process. After exposure, the wafer is baked at 95^{o}C before it's dipped into developer. Finally, the oxide layer underneath the PMMA is etched anisotropically using high density plasma etcher. The etched layer in the oxide will become the source, drain and nanowire of the SET (Figure 8(d)).

After define the source, drain and gate region is defined, a 60 nm thick Poly-Silicon is then deposited on the gate oxide. Then, the second mask (Figure 4) is transferred on the gate oxide layer using the e-beam lithography process (Figure 8(e)). After the unmasked region is etching, the polysilicon gate is formed on the gate oxide layer (Figure 8(f)).

Next, another lithographic step (Figure 8(g)) is used to pattern the oxide layer creating contact holes through which the aluminum probe pads contact the silicon. Once the contacts are opened (Figure 8(h)), a 200 nm aluminum is evaporated onto the entire surface of the wafer using the aluminum PVD module. A final lithographic step (Figure 8(i)) is used to pattern the probe pads and interconnections. Then, the final structure of SET is shown in Figure 8(j).

Ultimately, this project is targeted to produce SET device with a nanowire length and nanowire width of approximately 0.100 μm and 0.010 μm respectively. Our existing CMOS process coupled with E-beam lithography and high density plasma capability enables to achieve the project a more realistic target.

5. SET process and device simulation

Process and device simulation is commonly use for the design of new very large scale integration (VLSI) devices and processes. Simulation programs serve as exploratory tools in order to gain better understanding of process and device physics [24]. By using technology computer-aided design (TCAD) tools, an efficient virtual laboratory can be setup to minimize the usage of time and allow a variety of projects to be assigned [25]. The simulation of the fabrication (process simulation) and the electrical properties of devices (device simulation) and partly also circuits (circuit simulation) constitutes the area of TCAD [26].For process and device simulation, Synopsys TCAD tools TSUPREM-4 [27-28] and MEDICI [29-30] is used.

Mask layout is an input data for process simulation. The mask layout consist of four mask layers specially source layer, polysilicon gate layer, contact layer, and metal layer. These mask layout is designed using Taurus Layout from Synopsys TCAD. The complete mask layout for SET is shown in Figure 9.

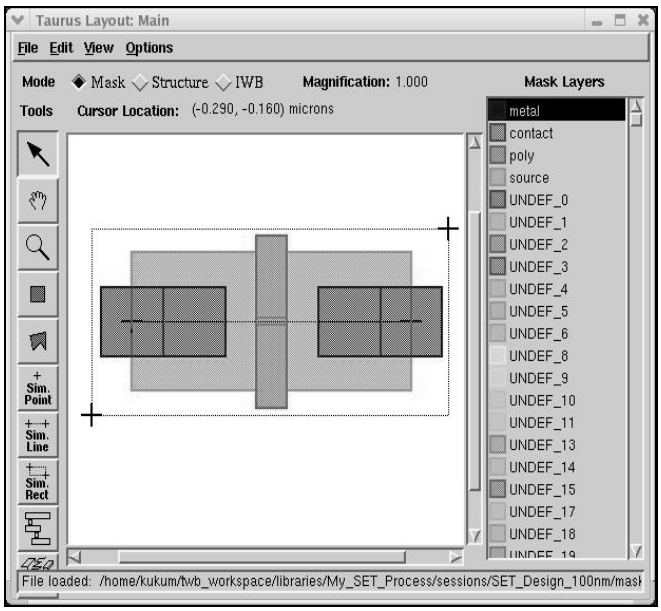

Fig. 9: Mask layout for SET simulation designed using Taurus Layout.

From Figure 9, the layout is selected as a linear cut in a full layout for a two-dimensional simulation or a rectangular cut from the layout for a three-dimensional simulation [31].

The process simulation is to define the SET device structure and process parameter. After completed the process simulation, the device structure of SET is shown in Figure 10.

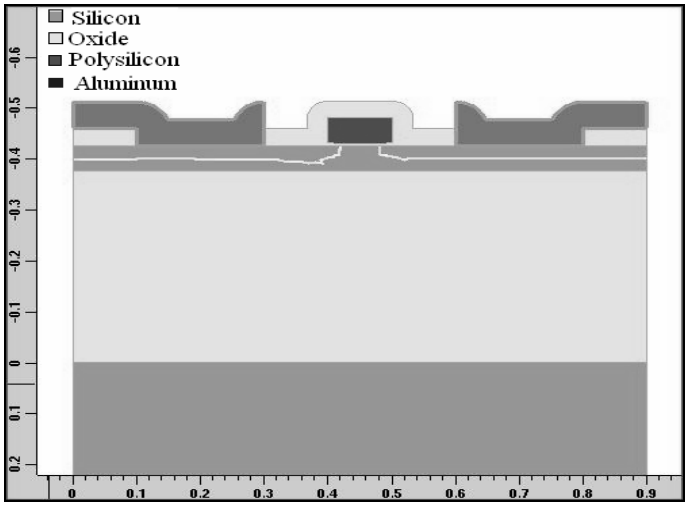

Fig. 10: Cross-section view of the device structure after completion of metallization process.

The structure is next annealed at 450 ^{o}C for 30 seconds. The four electrodes such as source, drain, gate and substrate is defined. Once processing is completed, the finished structure (full transistor) is saved and will be used in Taurus Medici for device characteristics.

After completion of the two-dimensional simulation, the three-dimensional simulation is done by using the Taurus Davinci. The results from this simulation are shown in Figure 11.

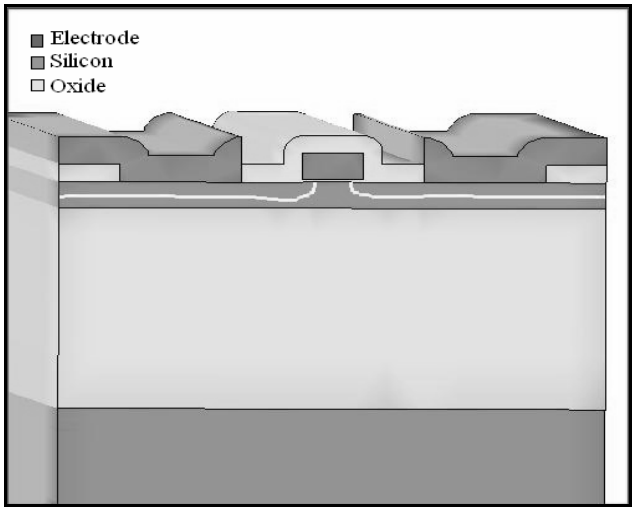

Fig. 11: Three dimensional structure of SET device.

Then, the device characteristics of SET device are simulated employing Taurus TSUPREM-4 (process simulator) and Taurus Medici (device simulator). For gate characteristic, the drain current, I_D as a function of the gate voltage, V_G is shown in Figure 12, for the SET made of silicon nanowire with a design length of 100 nm.

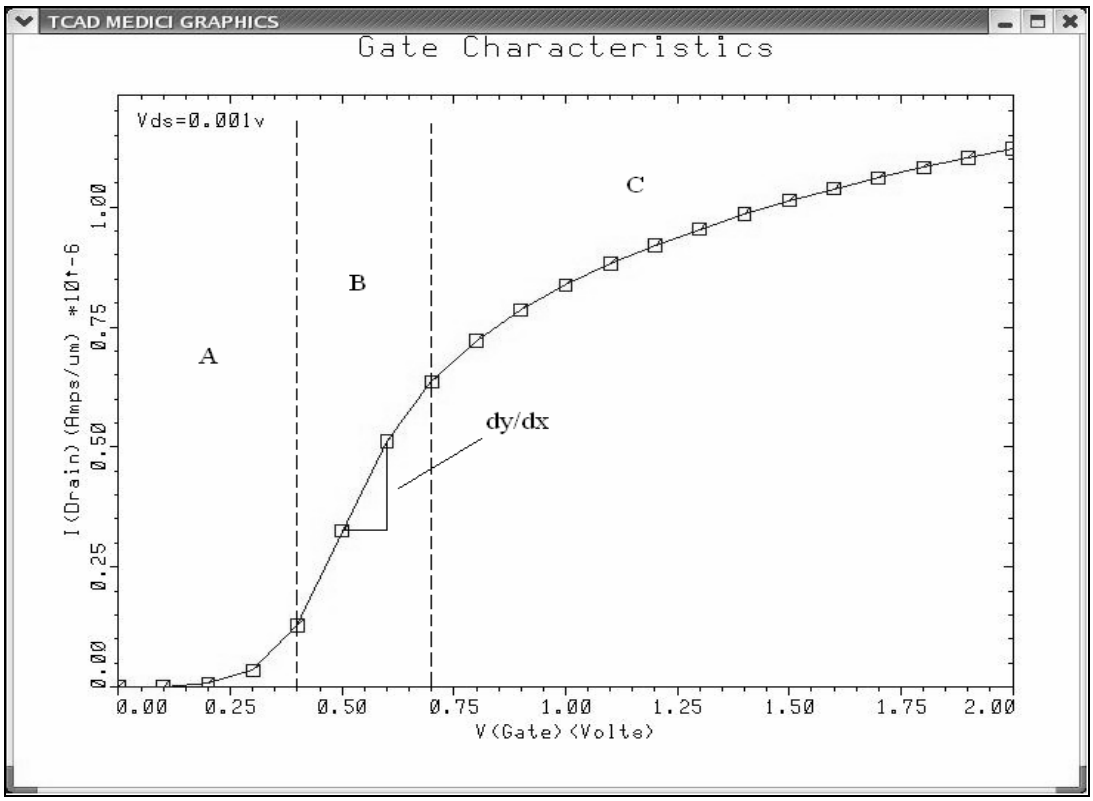

Fig. 12: Drain current, I_D as a function of the gate voltage, V_G.

Here, the drain voltage was 1 mV, the source and substrate (back gate) voltages were fixed at 0 V and the device temperature was 300 K or 27 ^oC (room temperature).

As shown in Figure 11, the graph is divided into three sections. In section A (from V_G at 0 V to V_G = 0.4 V), the drain current is increased immediately. At V_G = 0. 4 to V_G = 0.7 V (section B), the drain current increased linearly. While, in the section C when V_G is 0.7 V to 2.0 V, the drain current increased slowly.

Additionally, this graph is also given some information about this device. Firstly, the linear slope of this exponential graph is calculated. The linear slope is given by

$$\frac{dy}{dx} = \frac{y_2 - y_1}{x_2 - x_1} \tag{5.1}$$

From the I_D-V_G graph (Figure 12),

$$\frac{dy}{dx} = \frac{(5.2166 \times 10^{-7} - 2.8302 \times 10^{-7})A/\mu m}{(0.6 - 0.5)V} = 2.3864 \times 10^{-6}\, A/\mu mV$$

From this calculation, the linear slope is 2.3864 x 10^{-6} A/μmV. From the Ohm law,

$$V = IR, \tag{5.2}$$

the resistance, *R* of SET device can be calculated. Based on the Ohm law, the resistance, *R* is

$$R = \frac{V_G}{I_D} = \frac{1}{\frac{dy}{dx}} = \frac{1}{\left(2.3864 \times 10^{-6}\right) \times 0.1\mu m}\, \mu mV/A = 4.1904 \times 10^6\, \Omega$$

From the calculation, the SET device resistance, R is 4.1904 x 10^6 Ω. The power, P of SET device is given below,

$$P = VI \tag{5.3}$$

From Equation (5.2), $V = IR$, so the power is

$$P = I^2 R \tag{5.4}$$

From I_D-V_G graph as shown in Figure 5.25, let say I = 3.0 x 10^{-7} A/μm hence

$$P = [(\frac{3.0 \times 10^{-7} A}{\mu m} \times 0.1 \mu m)^2] \times [4.1904 \times 10^6 \Omega]$$
$$P = 3.771 \times 10^{-9} Watt$$

The power, P for SET device is 3.771 x 10^{-9} Watt for a fixed current. If voltage is fixed, let say V = 0.5 V, I = 2.8302 x 10^{-7} A/μm (get from Figure 5.25) and R = 4.1904 x 10^6 Ω,

$$P = [(\frac{2.8302 \times 10^{-7} A}{\mu m} \times 0.1 \mu m)^2] \times [0.4190 \times 10^6 \Omega]$$
$$P = 3.3565 \times 10^{-9} Watt$$

So, power, P =3.3565 x 10^{-9} Watt. From the two calculations of power, the power, P of SET device is very low (10^{-9} Watt).
Based on the literature review (Chapter 2), the threshold voltage, V_{TH} is

$$V_{th} = \frac{e}{C} \tag{5.5}$$

From Equation (5.5), the capacitance, C of SET device can be calculated. From the I_D-V_G graph, V_{TH} = 0.3728 V at V_G = 0.5 V and e = 1.602 x 10^{-19} C. Hence, the capacitance, C is

$$C = \frac{e}{V_{TH}} = \frac{1.602 \times 10^{-19} C}{0.3728 V} = 0.4297 \times 10^{-18} F$$

The calculation showed capacitance, C = 0.4297 x 10^{-18} F or 0.4297 aF. As a result, the capacitance, C from the simulation result is 0.4297 aF at 300 K. Based on the previous experimental result done by Wasshuber, the capacitance, C is 3 aF at 300 K [32]. An other result done by Takahashi *et.al.* [33] is C = 2 aF at room temperature. Compare to two of the three results, the result from the simulation is smaller than the previous experiment done by others.
The charging energy, E_C for SET is given below,

$$E_C = \frac{e^2}{2C} \tag{5.6}$$

From Equation (5.5), C = 0.4297 x 10^{-18} F. Hence, the charging energy for this system is

$$E_C = \frac{(1.602\times10^{-19})^2}{2(0.4297\times10^{-18})}$$

$$E_C = \frac{2.9863\times10^{-20}}{1.602\times10^{-19}}eV$$

$$E_C = 0.1864eV = 186.4meV$$

The calculation showed the charging energy, E_C for SET system is 186.4 meV at 300 K. Based on the previous reported about SET [34]; the charging energy is increased to 173 meV, which means that the transistor is able to operate at 300K. As a result, the value of charging energy from this calculation is nearly to the previous reported. Hence, the SET in this project is operated at 300 K.

In addition, the threshold voltage at 0.600 V gate bias is 0.3728 V and the channel length of the SET device is 61.27 nm. The simulation result shows that the sub threshold slopes for SET at 0.10 V gate bias is 112.3 mV/decade. The leakage current (I_{OOF}) at 0.0 V gate bias is 4.1715×10^{-12} A/μm. The drive current, I_{ON} is 0.034 μA/μm at $V_G = V_D = 1.5$ V.

Conclusion

Among various single-electron devices (SEDs), the single-electron transistor (SET) is the most fundamental. The SET masks were successfully designed using ELPHY Quantum GDS II Editor Offline Software of Raith EBL system. The SET masks consists of four masks namely source and drain mask, polysilicon gate mask, contact mask and metallization mask. The spacing between the source and drain is called nanowire. Nanowire is designed with a length and width approximately 100 nm and 10 nm respectively. Recently, the process flow developments of SET consists of four major processes which are source/drain and nanowire formation, polysilicon gate formation, contact formation, and metallization. In this study, Synopsys TCAD simulation tools are utilized for process and device simulation of SET. The simulation results showed the two-dimensional structure of SET from process simulation by using Taurus TSUPREM-4, the three-dimensional structure of SET from three-dimensional simulation by using Taurus Davinci and SET device characteristics from device simulation by using Taurus Medici.

From the simulation, the threshold voltage for SET device is 0.3728 V and the channel length is 61.27 nm. The SET device is operated at 300K (room temperature operation). From the calculation, the charging energy, E_C of SET system is 186.4 meV. The capacitance, C of SET device is 0.4297 aF and the power, P of SET device is 3.771 x 10^{-9} Watt for fixed current and 3.3565 x 10^{-9} Watt if fixed the gate voltage. The power, P of this SET device is obtained from the I_D-V_G graph with fixed the resistance, R. The resistance, R is 4.1904 x 10^6 Ω. The value of capacitance that obtained in this simulation is smaller than the previous experiment and the charging energy is higher than the previous reported. Ultimately, this research has utilized the process and device simulation tools as an alternative for an actual SET fabrication process.

Acknowledgement

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