FET with underlap structure for biosensing applications

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Abstract— **This paper presents the numerical simulation of an underlap field effect transistor (FET) device architecture on silicon-on-insulator (SOI) substrate for biosensing applications. By using the Silvaco ATLAS device simulator, this work is aimed to elucidate the effects of the different gate lengths, the presence of interface charge on the underlap sensing region, and also the effects of different gate biases (i.e. singlegate biasing, synchronous doublegate biasing and asynchronous doublegate biasing) on the magnitude of drain current (I_D) of the simulated device. It is found that shorter gate length with the positive charges (on the n-p-n structure), at the sensing channel area increased the electron concentration at the channel and substrate/buried oxide interface. In asynchronous doublegate with a +3V of back-gate supply and synchronous double-gate, both increased the I_D at different magnitude level and off-current. Thus, depending on the biomolecule charges, the substrate biasing can be altered to improve the device's sensitivity.**

Keywords— *Underlap field-effect transistor; biosensors; singlegate; synchronous doublegate ; asynchronous double-gate biasing.*

I. INTRODUCTION

A biosensor transforms physical or chemical changes accompanying biological reaction into an electrical signal. Typically, a biosensor has two elements, which are bio-receptor and transducer. Bio-receptor is an immobilized sensitive biological element that recognizes the analyte such as an enzyme, antibody and deoxyribonucleic acid (DNA). On the other hand, a transducer is used to convert the biochemical signal from the result of interaction between the analyte and bio-receptor, into another form of readable signal. These transduced signals vary according to the concentration of analytes being detected in the solution [1], [2].

The semiconductor-based biosensor configuration based on field-effect transistor (FET) device is often used due to its powerful platform for the direct detection of biological and chemical species [3], [4]. FET-based biosensors have high scalability, mass reproducibility, and compatibility with the on-chip integration on both the sensor and measurement system [5]. Various device architectures have been demonstrated at the device level [6], [7], [8] . In the so-called ion-sensitive FET (ISFET) based biosensor, the metal gate of the FET is replaced by a bio-film layer material. Drain current will change due to the bio-modulated gate surface, known as the 'gating effect' that influences the channel conductivity of the device. ISFET biosensor offers an outstanding architecture as compared to other devices in term of for use in high sensitive measurements, portable instrumentation, easy operation with a small amount of sample, low cost with mass reproducible and high speed [9].

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In order to overcome the problems of low binding probability in a carved nanogap and low structural stability stemming from the mechanically suspended nanogap structure, the FET with underlap structure is used. Biomolecules in underlap structure have a higher probability to bind to a designed area [10]. Besides that, the channel potential will be very sensitive to external charges in the underlap structure. Therefore, current change can be observed more precisely. The targeted molecules can be easily detected electrically by detecting the changes in the drain current [11]. Moreover, the combination of highly sensitive underlap FET structure with the presence of back-gate biasing is expected to further enhance the sensitivity of the device, boosting a low limit-of-detection (LOD) of the analyte molecules. With the implementation of double gate [12], [13],[14] it should be expected to enhance the sensitivity as demonstrated on device level [15].

In this paper, we simulate the underlap FET structure with a novelty of having an underlap as the transducing region for the bio-molecular recognition site. The paper is expected to explain the significance of different gate length on the device's electrical responses (I-V), besides analyzing on the impact of singlegate, synchronous doublegate and asynchronous doublegate towards the electrical properties of the proposed device structure for biosensing applications.

II. METHODOLOGY ON DEVICE SIMULATION

Device's Substrate

The simulations have been carried out utilizing ATLAS device simulation software. The device modelling structure was based on silicon-on-insulator (SOI) substrate with the thickness of the top p-type silicon layer of 70 nm, the thickness of the buried oxide (BOx) layer of 145 nm, and the bottom bulk silicon substrate with 100 μm thick respectively [16]. The main reason we are using SOI as substrate is due to its good electrostatic control on the transistor device channel. Besides that, it also has the ability to co-integrate devices on SOI with other devices on silicon bulk by etching the top silicon layer and the underlying BOx layer. Fig. 1 illustrates the top view and side view of simulation device model with the presence of underlap region between the gate-drain terminals.
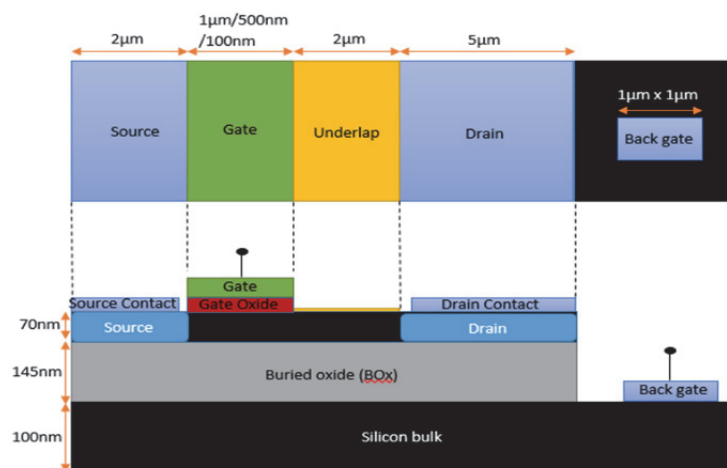

Fig. 1. Top view and side view of device model structure with an underlap region on an SOI.

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Device Model's Designing

The top 70 nm silicon layer and bottom 100 μm silicon bulk were uniformly doped with p-type dopant at a concentration of $1x10^{15}$ cm^{-3}. However, the source and drain regions were uniformly doped with n-type dopant at a concentration of $1x10^{20}$ cm^{-3}. The contacts were all aluminum with work-function set at 4.6 electron-volt (eV) layered on the contact surface, forming a Schottky contact on each of the terminals. The gate oxide thickness was set at 10 nm, while underlap length was fixed at 2 μm between the gate-drain terminals. The length of source and drain terminals were fixed at 2 μm and 5 μm respectively. These parameters were kept constant throughout the device modeling and simulations. Table 1 shows the fixed parameters on the modeled device for simulation.

TABLE 1. SIMULATION DEVICE'S FIXED PARAMETERS

Modelled Device's Dimensions	
Parameters	*Dimension value*
Silicon-on-insulator (SOI)	Top Si bulk: 70 nm Box: 145 nm Bottom Si-bulk: 100μm
Gate oxide thickness	10 nm
Underlap length	2 μm
Source length	2 μm
Drain length	5 μm
Back-gate length	2.5 μm
Source/drain doping	n-type at $1x10^{20}$ cm^{-3}
Undoped region	p-type at $1x10^{15}$ cm^{-3}
Interface charge	$6x10^{10}$ cm^{-2}

The simulated gate lengths were 1 μm, 500 nm and 100 nm with different interface charges, i.e. positive, negative and without interface charge on the underlap region. The interface charge represents the biomolecule charges. For example, DNA always carries negative charge due to its negatively charged phosphate backbone, meanwhile, proteins can be either positively or negatively charged, depending on its isoelectric point (pI). These design parameters were then simulated under the effect of singlegate biasing, synchronous doublegate biasing and asynchronous doublegate biasing to analyze the interactions between them. Table 2 shows the lists of simulation variables under test on the modeled device.

TABLE 2. DEVICE'S SIMULATION VARIABLES

Manipulative Variables	
Device's design and architectures	*Tested variables*
Interface charge on the underlap surface	Positive, negative and without interface charge
Gate length	1 μm, 500 nm and 100 nm

Manipulative Variables	
Device's design and architectures	*Tested variables*
Type of gate biasesSingle-gate, synchronous doublegate and asynchronous doublegate with +3V back-gate supply	

Device's Simulation Parameters

For single-gate, synchronous doublegate and asynchronous doublegate biases, the gate voltage was biased at +1.5 V under voltage step of +0.02 V. However, the back gate terminal of the asynchronous doublegate was biased at +3V under voltage step of +1.0V. The drain for all the three types of biasing was biased to +1.0 V under +0.1 V of voltage step.

III. RESULTS AND DISCUSSION

Fig. 2 shows the current – voltage (I-V) characteristics for different gate length when the device is in single biased (only top-gate is biased from 0 to 1.6 V). As expected, the 500 nm gate length has a better performance with better trade-off between on-state and off-state current compared to higher 1 μm and 100 nm gate length. This is due, longer gate introduced parasitic resistance between the source and drain terminals. This phenomenon restricts the formation of inversion layer when the gate voltage was applied, thus reducing the I_D. While for 100 nm length, the gate is losing control of the channel, thus increase the off-state current. At this gate length, it forms a weak inversion region between the source and drain. As the gate length is reduced, the capacitive coupling of the channel potential to the source and drain increases relative to the gate, leading to significantly degraded short-channel effects (SCE) which caused by the Drain-Induced barrier lowering (DIBL). It happened due to impact of drain electric field because of high drain voltage application when the potential barrier height for channel carriers at the edge of the source decreases [17].There is no current flow through when negative interface charge and no interface charge is applied to the surface of the underlap region.

Fig. 3 shows the electron concentration along the channel (Fig. 3a), when the underlap structure area is subjected for different charges (positive, negative and no charge). Initially, the channel is doped with n-type impurities. At the area underneath the channel region, the electron concentration changes from low to high concentration when the underlap is positively and negatively charged, respectively. Higher drain current can be obtained the positive charge due to an increase of electron concentration at the channel. Therefore, the conducting layer of mobile electrons formed at the Si surface beneath the oxide can carry current between the source and drain, through the channel.
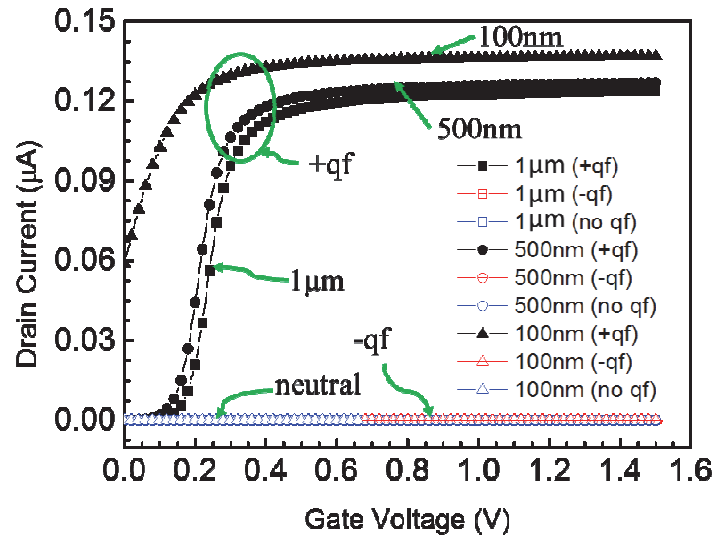
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Fig. 2. The effect of different gate length toward positive, negative and without interface charges at singlegate biasing
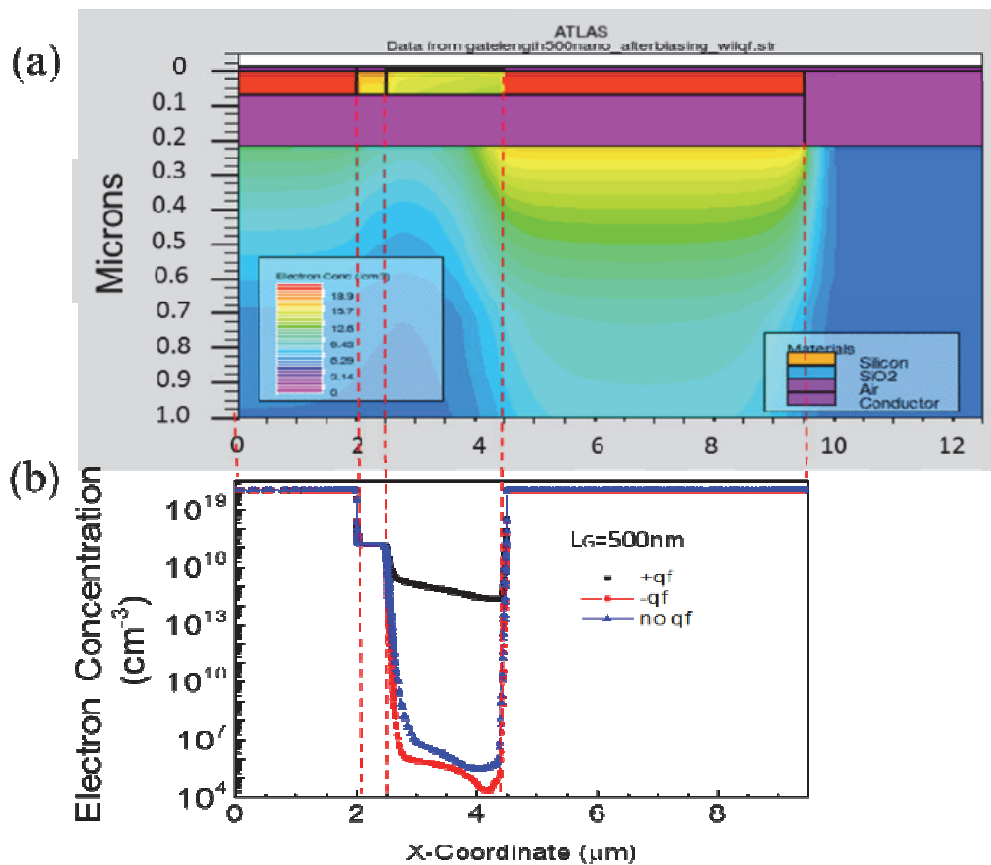

Fig. 3. (a) Tonyplot of the FET structure (b)Electron concentration along the channel

Fig. 4 shows the current – voltage (I-V) characteristics for different gate lengths when subjected to synchronous doublegate biasing. In synchronous doublegate, the front gate is connected with the back-gate, utilizing only one voltage supply. We can see

that, for 500 nm gate length with a synchronous doublegate and a positive interface charge at the sensing area has significantly increased the I_D compared to singlegate operation as discussed previously (Fig. 2). As for the 100 nm gate length, it has leakage current for all the three situations. The result of this reduction is the increment of injected carriers into the channel from the source that leads to the off current enlargement. Thus, it is not suitable for the use of biosensing application and not interesting to focus in the discussion.
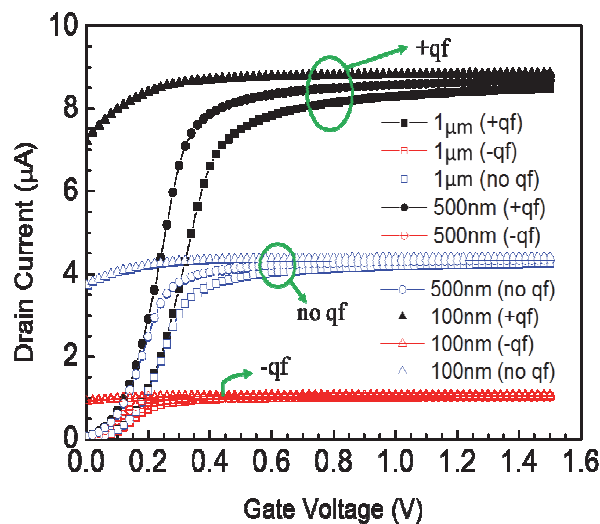

Fig. 4. The effect of different gate length with positive, negative and without interface charge at synchronous doublegate biasing

Fig. 5 shows the asynchronous double-gate biasing. At this condition the back-gate is supplied with +3 V voltage. One can see that, the increase of drain current is higher than single and synchronous doublegates, but at the expenses of high off-state current. This occurs at all interface charges condition, i.e. positive, negative and no interface charge.
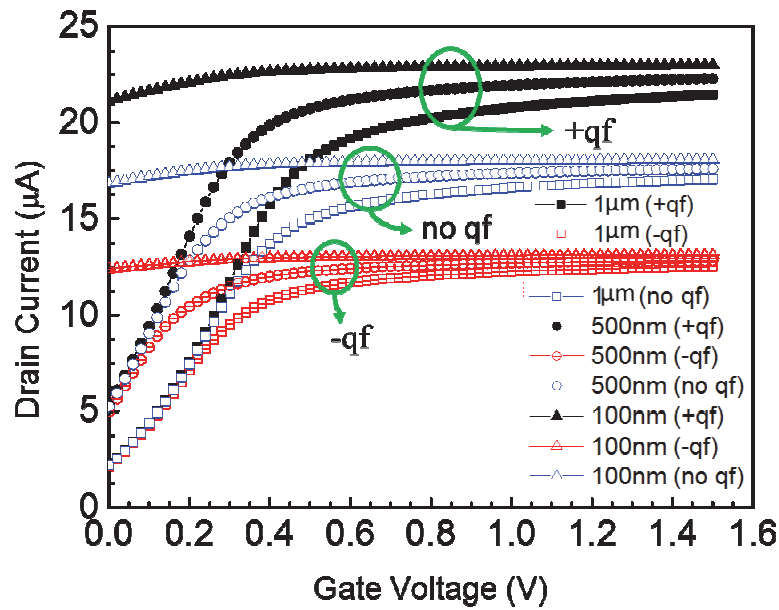
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Fig. 5. The effect of different gate length with positive, negative and without interface charges of asynchronous double gate, V_{bg} = +3 V.

Fig. 6 summarized the performance of 500 nm gate length for different voltage biasing condition. i.e. singlegate, synchronous and asynchronous doublegates with positive interface charge condition. The drain current increased significantly with asynchronous double-gate biasing. The increased is about 100 % and 200 % as compared to synchronous and singlegate biasing respectively. The drawback of synchronous back-gate biasing is the off-state current also increased.
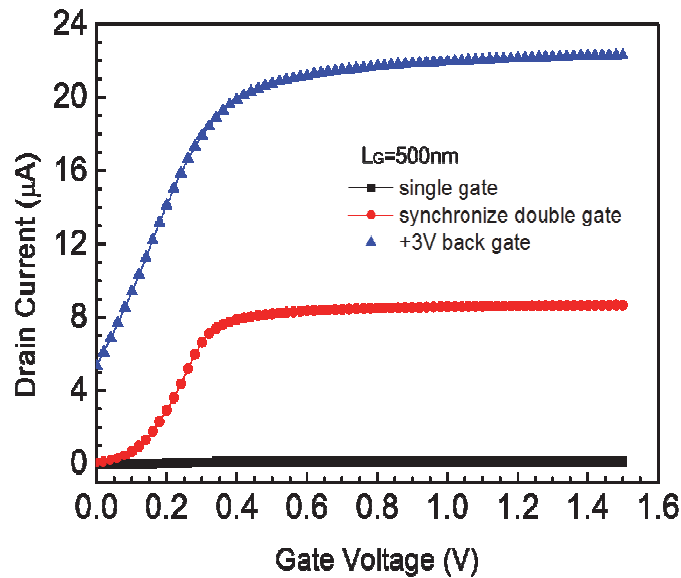

Fig. 6. Drain current characteristic for 500 nm gate length with singlegate, synchronous doublegate and asynchronous 3 V back-gate biasing.

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Fig. 7 shows the electron concentration for the result obtained in Fig. 6. The electron concentration cut is done at the middle of the channel (Fig. 7a) and at the substrate/BOx interface (Fig. 7b). At the channel area, the electron concentration is high under the asynchronous +3 V back-gate supply and a synchronous doublegate as compared to singlegate. Higher electron concentration at the channel can also be meant that the drain current flow between the terminals of source and drain also will be high. While at the substrate/BOx interface, higher concentration is observed with singlegate. As seen at the channel area, no significant difference in the electron concentration is observed between the synchronous double-gate and asynchronous double-gate biases (Fig. 7c).
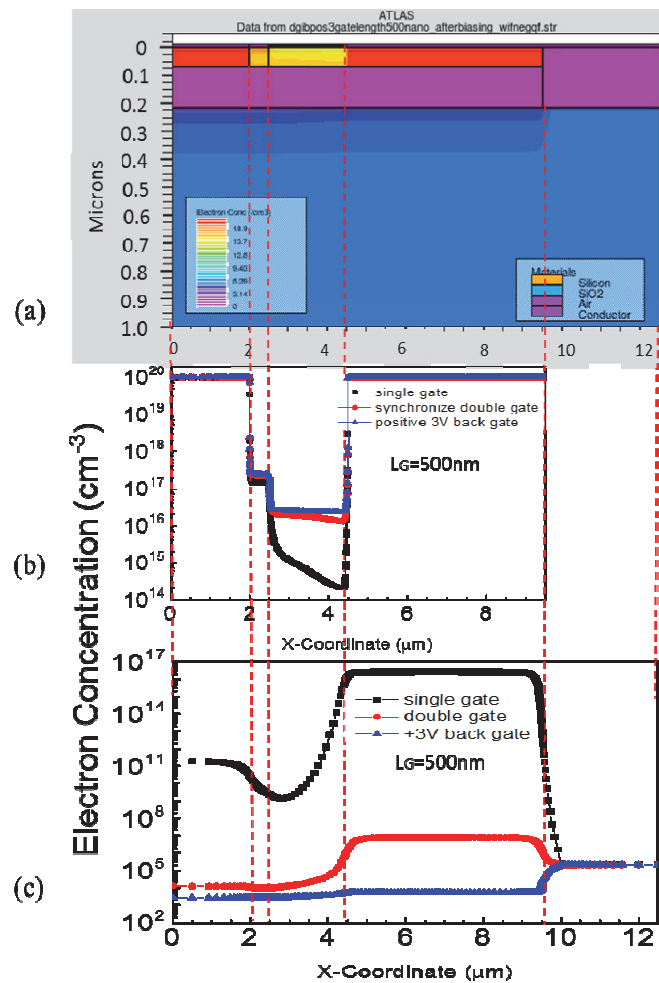

Fig. 7. Electron concentration for 500 nm gate length in different biasing along the terminals

IV. CONCLUSION

The simulated results on n-p-n junction, between source, channel and respectively, show that positive interface charge (which is translated into the positively charged biomolecules) has the highest drain current compared to the neutral and negatively charged

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molecules of the device. The asynchronous doublegate with +3V back-gate supply generates the highest I_D among the three types of biasing. From the simulated data, it shows that the presence of underlap structure in FET with either synchronous or asynchronous double-gate with +3V biasing enhances the I-V responses (i.e. exhibits high sensitivity for low to high concentration of analyte on the underlap 'sensing' surface) of the device. However, the synchronous doublegate device provides better trade-off performance between an on-state to off-state current as compared to the asynchronous +3 V back-gate biasing. Therefore, the findings show that underlap FET architecture holds an unprecedented potential to be used as a highly sensitive biosensors.

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