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A Survey on Emerging Technologies and Architectures of Low Power Preamplifiers for Biomedical Applications

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Abstract: Unlike other commercial devices, developing implantable microsystems for biomedical applications requires critical analysis in terms of specifications, technologies and design techniques because of the devices' safety and efficacy. As the industry of the medical implantable devices develops, lowering the power consumption as much as possible is essential in improving the service time of the battery, which cannot be replaced frequently. Hence low power design has become the main concern for battery-powered implants. Biosignals such as EEG, ECG are weak signals typically ranging from 0.5µV to 5mV with high source impedance and superimposed high level interference and noise. Hence there is a need of a pre-amplification stage in the analog front end of a biomedical acquisition system so that these biosignals can be amplified for measurement and testing purposes, without degrading the signal-to-noise ratio. The purpose is to provide amplification selective to the physiological signal and reject noise and other sources of interference. In this paper an in-depth study of various low power pre-amplifiers proposed for different biomedical applications has been done along with the performance comparison in terms of the various amplification related specifications such as gain, bandwidth, signal-to-noise ratio, CMRR, slew rate among others.

Keywords: Biomedical implants, Preamplifier, Low Power electronics, Analog Front End

Introduction

The term implant represents a medical device that acts as a part of the whole biological system or can be used to provide support to a damaged biological structure [1,2]. Currently biomedical implants are used for various applications including cardiac pacemakers, defibrillators, cardiovascular stents etc. Monitoring of biomedical signals provides us information about the vital health of body and thus the data can be of prime importance to medical practitioners [3]. With the rapid development in microelectronics towards medical therapies and diagnostic aids, there is a need for lowering the power consumption in active implantable devices that are battery powered so that the device lifetime increases. One such example of active implantable device is the Cardiac Pacemaker in terms of its widespread application [4]. A Cardiac Pacemaker is a device that uses electrical pulses to recover the normal heartbeat of a diseased heart. The major building blocks of the pacemaker, shown in Fig. 1, are analog front end (AFE) circuit, microcontroller with ultra low power consumption, battery and an output circuit that stimulates the heart. The AFE comprises of a preamplifier, low-pass filter, level shifter, synchronizing circuit etc [5]. The cardiac signal is given to a low noise preamplifier for amplification purposes and is then filtered. This filtered signal is then given to comparator that produces a pulse which depends upon the threshold voltage level. The output stage of a pacemaker is called a charge pump that uses a pulse generator to stimulate the activity of the heart. Thus a preamplifier is critical block that is used for the detection of the small level signals especially for the biomedical applications [3].

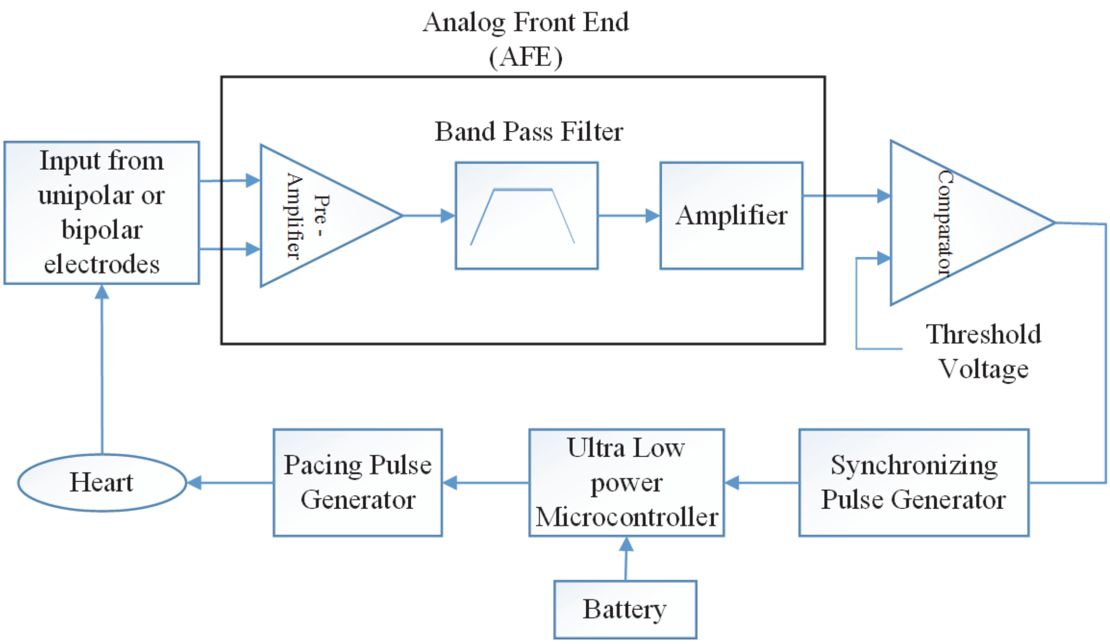

Fig. 1: Block diagram of a typical implantable cardiac pacemaker system

Need for Pre-amplification

The Biosignals like EEG, ECG, EMG, EOG are weak signals with input amplitude typically ranging from 0.5uV to 5mV [5,6] and are highly susceptible to noise and power line interference at 50Hz to 60Hz. Nowadays there is a demand for a low noise, low power bio acquisition system so as to avoid bulky connectivity and reduce patients' mobility and discomfort [7]. A Preamplifier is one of the important component of the analog front end as it determines the SNR of the entire biomedical signal acquisition system and is required for reliable monitoring of the physiological signal [8]. The weak biosignal needs to be amplified so that it is compatible with devices like displays, recorders, A/D converters, etc. and for measurement and testing purposes [9]. This paper presents a comprehensive study of different preamplifier topologies along with their performance comparison in terms of the various amplification related specifications such as gain, power consumption, common mode rejection ratio (CMRR) and input referred noise among others.

Low Power Preamplifiers in Biomedical Applications

Much of the research work is currently being done on neural implantable devices, cochlear implants etc. For neural applications parameters like low noise, low power are critical mainly because 1/f or flicker noise is more predominant at low frequencies [5] and some other sources of noise like from electrode tissue interface and EMG (generated by muscles) cause interference with the neural signal (ENG) of amplitude (10μV-500μV) and frequency (10Hz - 10KHz) [10]. The ENG signal has similar frequency band as that of 1/f noise and this in turn causes degradation of the SNR. Therefore it becomes important that the input referred noise of the amplifier should be minimized so as to boost the SNR. Also low power operation is considered important in order to minimize die area and to increase the battery lifetime. The amplifier should dissipate less power so that there are less chances of damaging the surrounding tissue by heat produced.

R Reiger et al. proposed a BiCMOS Neural preamplifier [10] and this is compared with CMOS operating in weak and strong inversion and it is shown that BiCMOS has the best 1/f noise performance. If same performance is to be obtained from CMOS process then power consumption will be more and there will be an increase in the device size, but the main disadvantage of using BiCMOS is its greater cost. Previously techniques like chopper stabilization, shown in Fig. 2, have been used to eliminate the 1/f noise [11, 12].

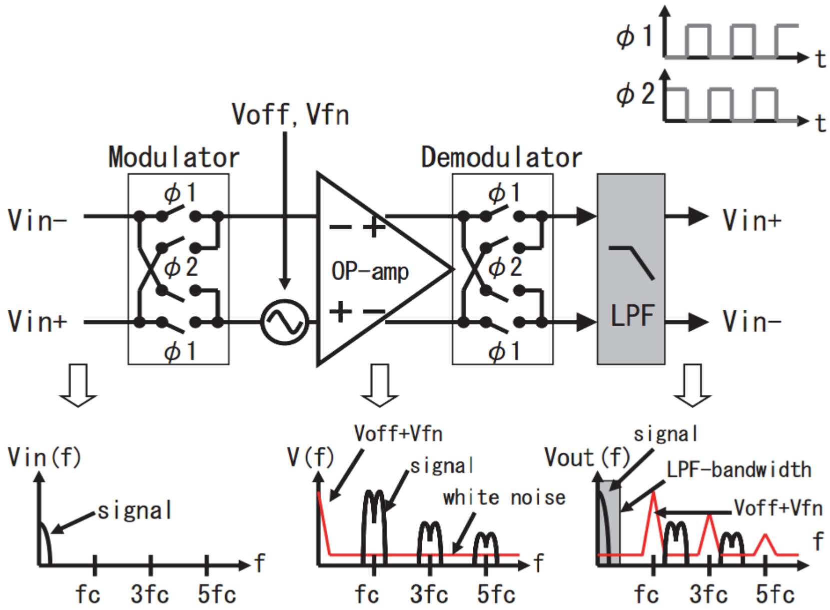

Fig. 2: Chopper stabilization Technique [12].

The main disadvantage of this technique is that there is a need for an amplifier operating at higher frequencies with higher power consumption (not desirable for the implant). Therefore improved techniques have been described, taking advantage of high g_m/I_d ratio of devices operating in sub-threshold [13] so as to achieve low noise, low power and best noise Efficiency factor (NEF) which describes noise power trade-off. The MOSFET operating in sub-threshold region has smaller current interference (trapping and detrapping of charge carriers) because carrier transfer mechanism is mainly due to diffusion current that is directed away from SiO_2 interface, hence flicker noise is smaller in sub-threshold region. But there are some stability concerns associated with these closed loop amplifiers that limits power noise efficiency hence open loop amplifiers have been proposed which have better noise performance but at the expense of linearity, reduced power supply rejection etc. [14]. A pseudo-open loop energy efficient amplifier, shown in Fig.3, with programmable bandpass has been designed that retains high linearity and stability [15].

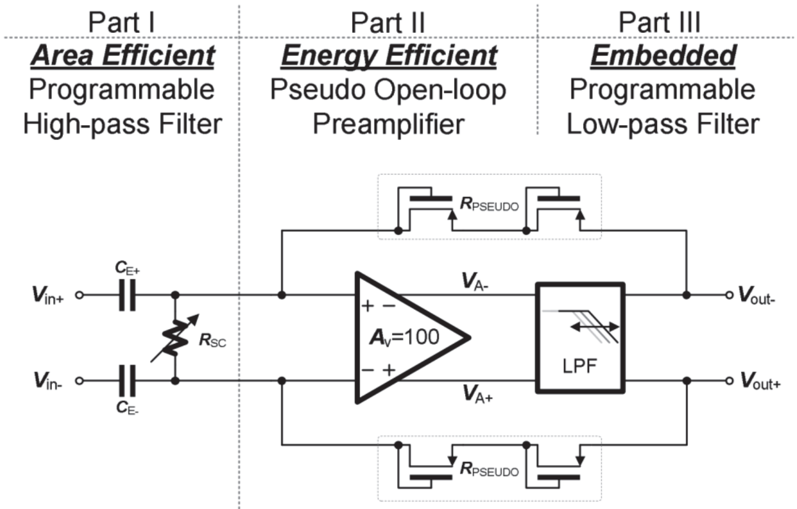

Fig. 3: Pseudo-open loop energy efficient preamplifier [15].

The current trend in the design of neural amplifiers aims at amplifying the local field potentials (LFP) (<100Hz) instead of spikes (100Hz-7KHz). Spikes convey information about the extracellular neural activity of a single neuron unit. In contrast LFPs convey information about neural activity recorded from ensemble of neurons. LFPs are useful in neuroprosthetic amplifiers and also help in interpreting specific motor activities, in understanding neurodegenerative pathologies. The main advantage of using LFPs is that it can be obtained directly from the raw signal. Also it can be measured in absence of spikes. The major constraints in LFP recording are power and area. In some applications these spikes and LFPs are separated to analyze them separately. Haddad et al. [16] proposed a true logarithmic amplifier (TLA), shown in Fig. 4, that amplifies low amplitude spikes with suitable gain (64.6 dB) in order to avoid separation of the LFPs and spikes while consuming less power (around 11µW). S. Dwivedi et al. presented a Single Ended OTA [17] with a DC shifting technique with ultra-low power consumption for LFP recording applications. It exhibits a wide dynamic range of 68dB and consumes a chip area of less than 0.10 mm^2 [17]. Presently the reduction in technology from 180nm to 45nm is also reported in the literature for neural amplifiers. With the use of current mode amplifiers [18] shown in Fig.5, there is a substantial improvement in parameter values like reduction in power consumption, supply voltage, noise etc. at 45nm as compared to 180nm.

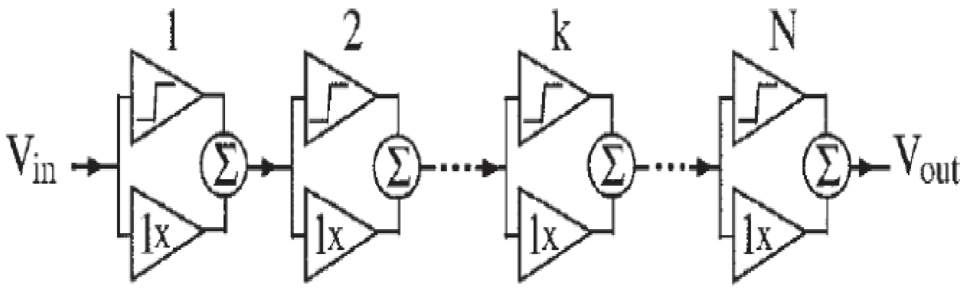

Fig. 4: TLA structure with cascaded dual gain stages [16].

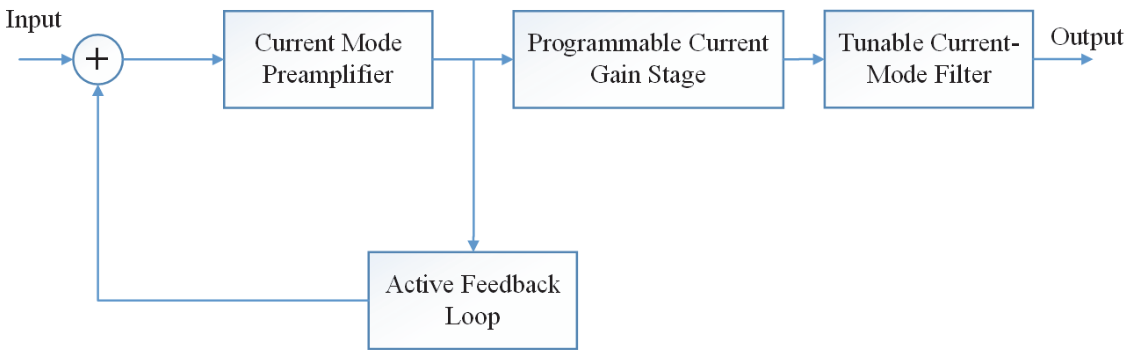

Fig. 5: Current Mode preamplifier.

Recently, analog front end for treatment of epilepsy through the technique of deep brain stimulation (DBS) is also reported [19]. One of the important characteristics of the front end for this particular application is that it must be able to monitor the prolonged periods of epileptic seizures while consuming ultra-low power. Also the noise power trade off must be maintained throughout the design. A folded cascode technique [19] is used that achieves a good noise-power tradeoff. To achieve low noise the quiescent current are minimized that do not contribute to the overall transconductance of the amplifier. The drawback is reduced slew rate which is not that important for this particular application. C.Qian et al. [19] proposed the technique of combining current splitting and output current scaling Fig.6 in order to get low OTA noise.

Another technique of folded cascode with current stealing [8] is used to achieve lower power consumption and achieves one of the best NEF 2.60 (lowest so far).

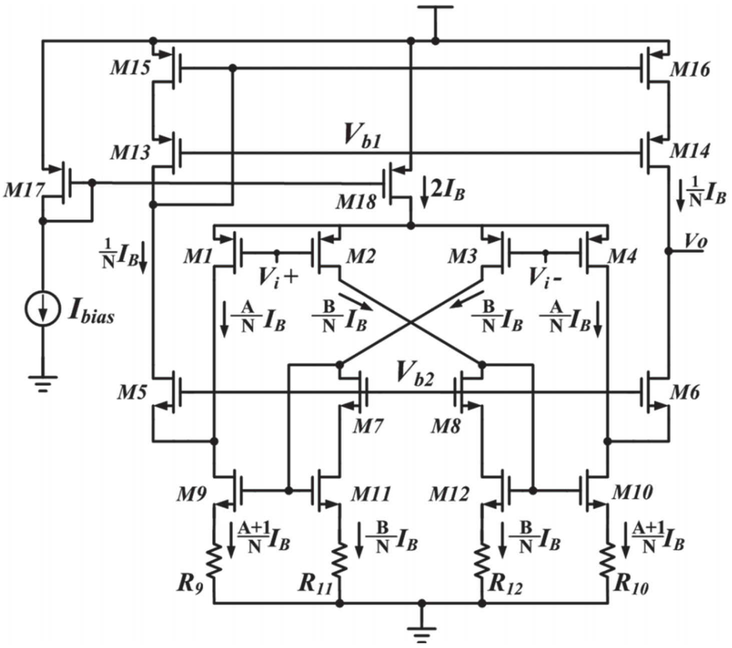

Fig. 6: Low Noise OTA with combined current scaling and splitting technique suitable for Epileptic seizure detection [19].

For the general biomedical applications which include multi-biosignals like (EEG, ECG, EMG, EOG) etc. parameters like high CMRR, tunable gain and bandwidth are desirable for amplifying the different biomedical signals besides low noise and low power. C.Huang et al. [20] proposed a novel analog front end integrated circuit (AFEIC) having a current balancing instrumentation amplifier (CBIA) for biomedical applications that achieves low noise, low power, high CMRR, high gain, high PSRR simultaneously. The gain is programmable from 52.6dB-80.4dB so as to amplify the various biosignals and the bandwidth is selectable. The advantage of using CBIA is improved CMRR because of high swing cascade current mirror used instead of a simple current mirror. Further techniques like current mode instrumentation amplifier, shown in Fig. 7 [21], have been used to amplify biomedical signal with high CMRR and configurable gain.

The main advantage of this topology is that CMRR remains almost constant in spite of changing differential gain. The major drawback of using instrumentation amplifier is that it has high power consumption and also requires too many resistors due to which the battery operating time is reduced and the area cost also increases. Thus R.Chebli et al. [7] proposed a technique of chopped logarithmic programmable gain amplifier (CPLGA), as shown in Fig.8, dedicated for

EEG acquisition systems that has several advantages over the conventional instrumentation amplifiers (IA) like high CMRR, PSRR, low noise, wide bandwidth, non-cross distortion, etc.

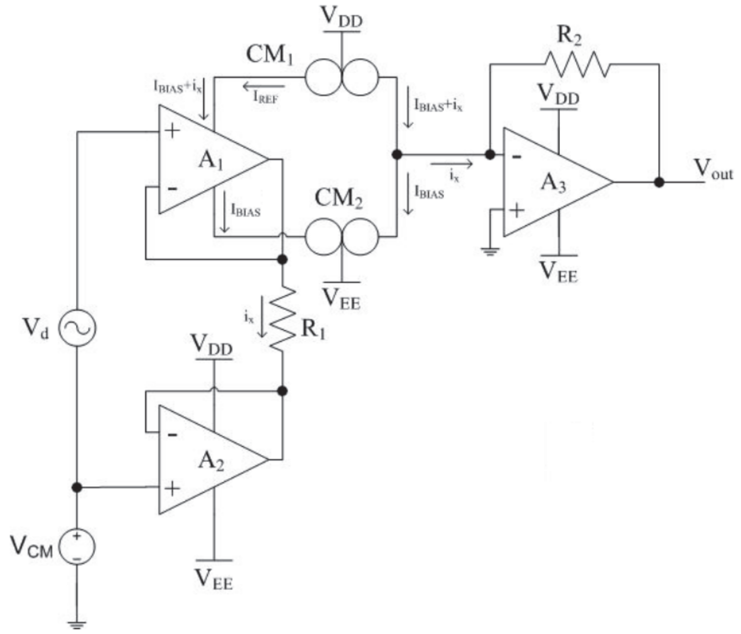

Fig. 7: Current Mode Instrumentation Amplifier (CMIA) [21]

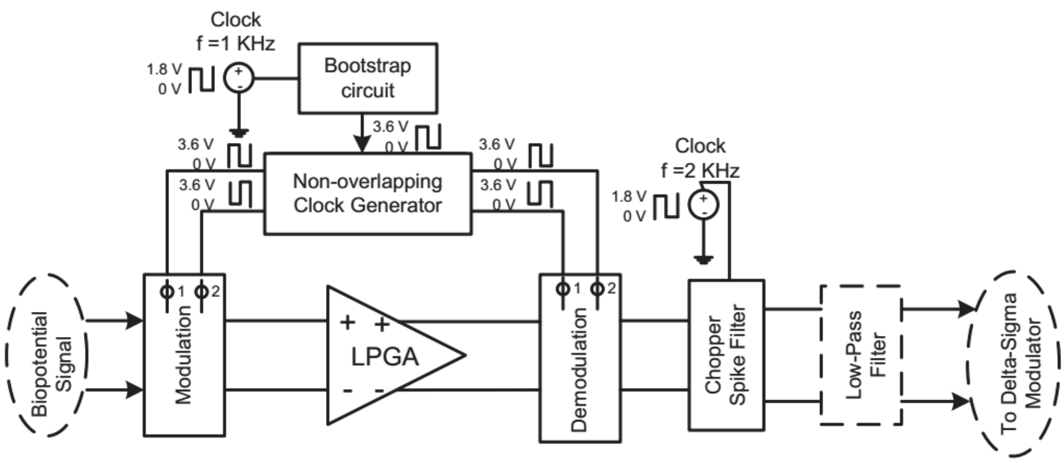

Fig. 8: Chopped Programmable Logarithmic Gain Amplifier (CPLGA) [7].

Much of the research is also done on cochlear implants. These bionic implants require a front end with wide dynamic range, minimum external components, low power and good PSRR. A high PSRR ensures that the analog-to-digital converter is not exposed to distortion errors and effects of aliasing that are mainly caused due to high frequency supply noise. The designs used previously had a custom external electret structure [22]. A technique of non-custom JFET buffered microphone is proposed in [23], as shown in Fig. 9, where the output current instead of its output voltage is transduced by using a sense amplifier topology and thus achieving a good PSRR. FET amplifiers reduce flicker noise but have several disadvantages like higher power consumption, limitations on SNR, need for external components

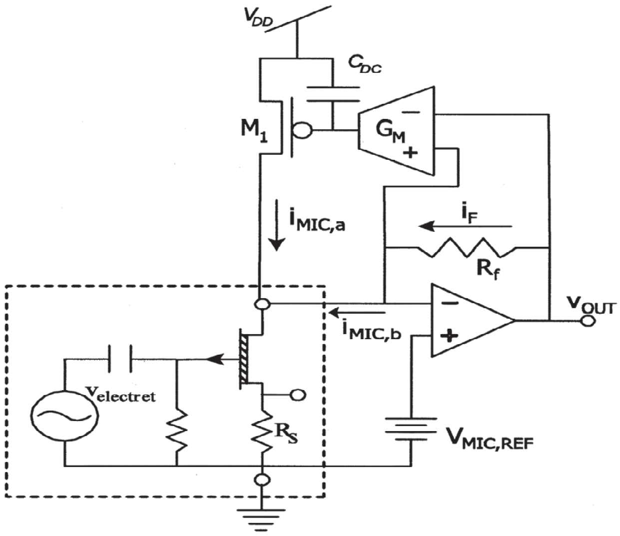

Fig. 9: Sense Amplifier Topology with Split frequency feedback [23]

Therefore a preamplifier is described [24] with improved biasing technique suitable for use in cochlear implants. A differential circuit with current mirroring, shown in Fig. 10, is used that achieves SNR of >80dB in frequency band of 100Hz-10KHz and a total harmonic distortion of better than >-55dB, is better compared to FET preamplifier with SNR of around 60-65dB. Also this does not need any external components and requires only two input pins.

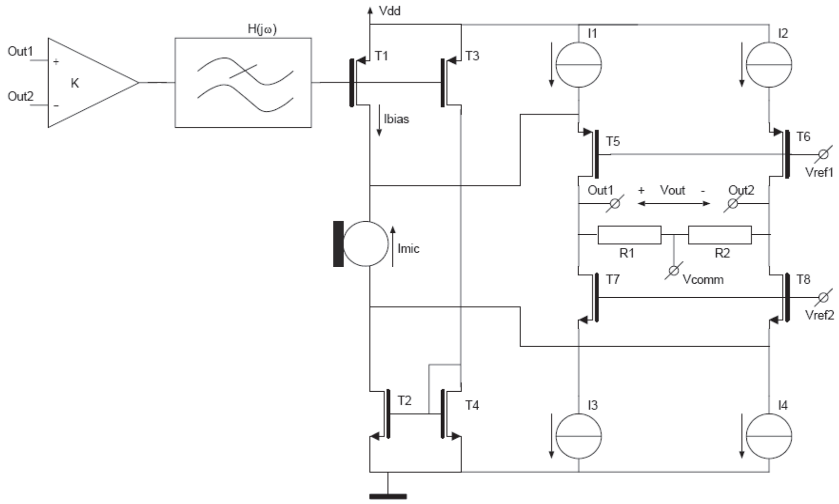

Fig. 10: Differential amplifier with Current Mirror [24].

For implantable ECG applications some parameters like size, weight, battery, and power consumption are of prime importance. M Burke et al. [25] described an instrumentation amplifier with low power consumption of 30µW from 3.3V for heart rate monitoring based on dry electrode recording and used for applications where long term monitoring of ECG is required. An analog front end for QRS detection [26] is presented with a current consumption of 600nA and a programmable gain of 36dB-56dB with a supply voltage ranging from 1.8-2.8V using 0.35um CMOS technology. Further an instrumentation amplifier with added Common mode feedback, shown in Fig.11 [27], for electrocardiogram applications is reported having less power consumption and achieving a CMRR of 90dB suitable for this particular application. CMRR becomes an important parameter here because of large amount of 60Hz hum in biopotential recording.

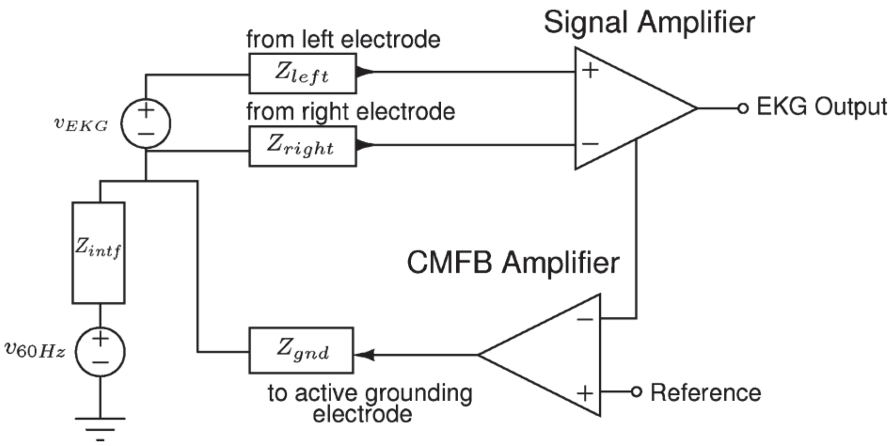

Fig. 11: Electrocardiogram amplifier with CMFB [27]

Discussion:

Neural implantable devices, EEG and Cochlear Implants cover a major portion of the survey while less explored applications being Cardiac Pacemaker, Deep Brain stimulation, Retinal Prostheses. The key design parameters of an amplifier are its Gain, stability, power consumption, CMRR, PSRR, Noise, THD, Dynamic range etc. Different applications demand different parameters that are critical to that particular application. Some applications like Neural Implantable devices require a low noise, low power analog front end while others like cochlear require a high PSRR, good SNR etc. The main parameters explored so far in the survey are Input referred noise, power consumption for neural implantable devices. The less explored parameters being, Input referred noise, output swing, THD, Dynamic range for ECG applications. The Input referred noise represents how much the input signal is affected by the circuit's noise. Thus it can be considered for ECG signal where 60Hz hum can cause interference with the ECG signal (0.05Hz-250Hz). Also Output swing becomes an important metric while we are considering reduced supply voltage. A large output swing allows input and output to be short circuited that makes it easier for selection of input common mode level.

The trends and various parameters obtained along with their comparison for different applications are shown graphically in figures 12-15.

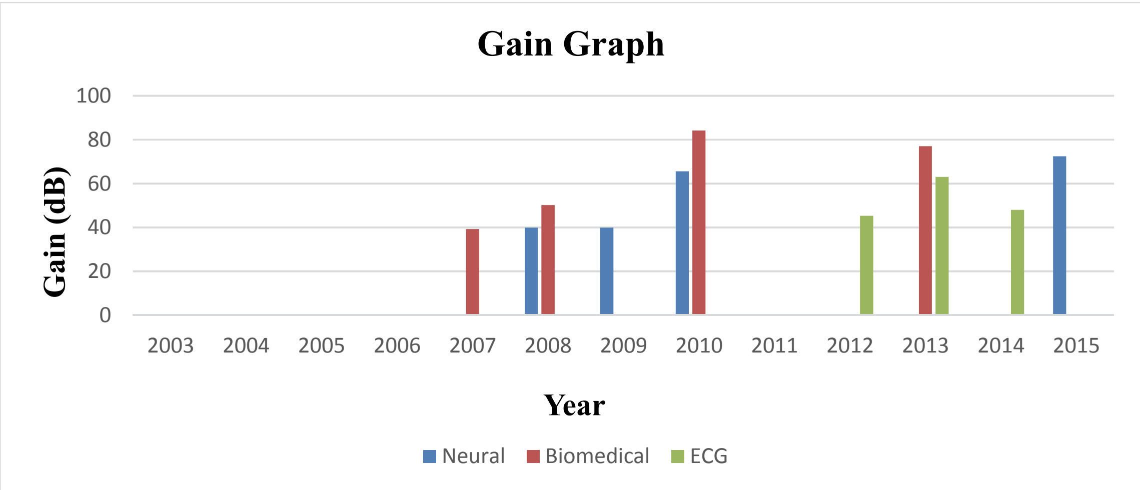

Fig. 12: Gain trend for various applications.

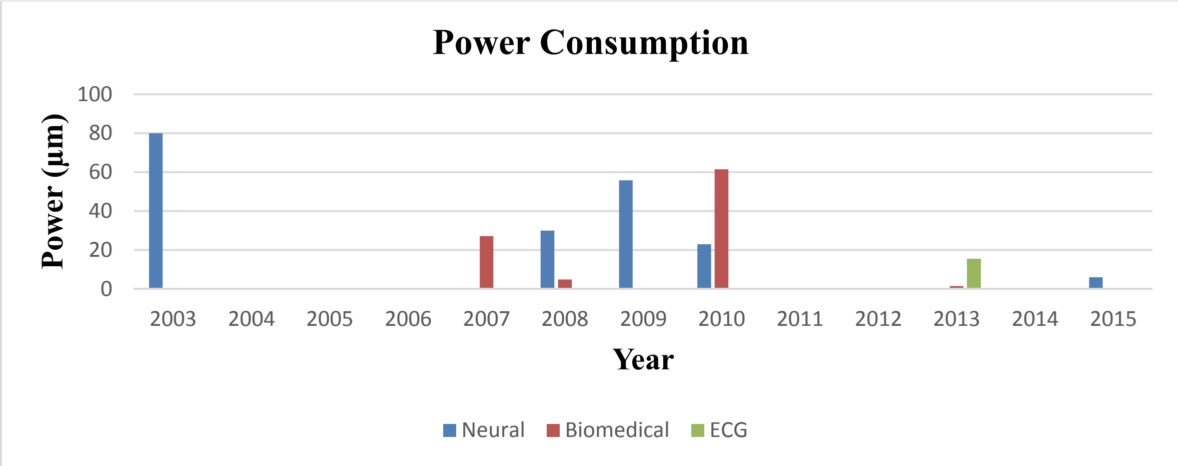

Fig. 13: Power Consumption trend for various biomedical applications

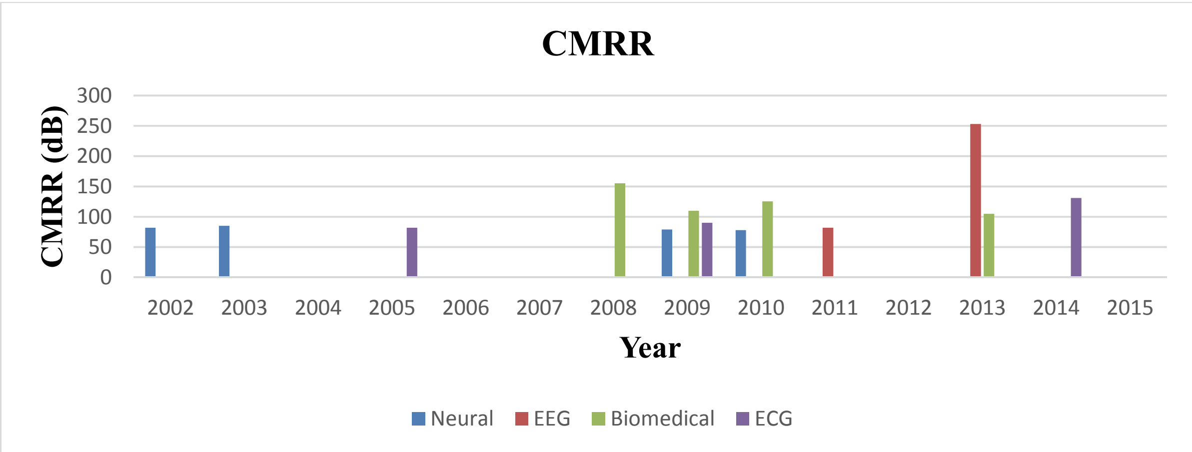

Fig. 14: CMRR performance trend for various biomedical applications.

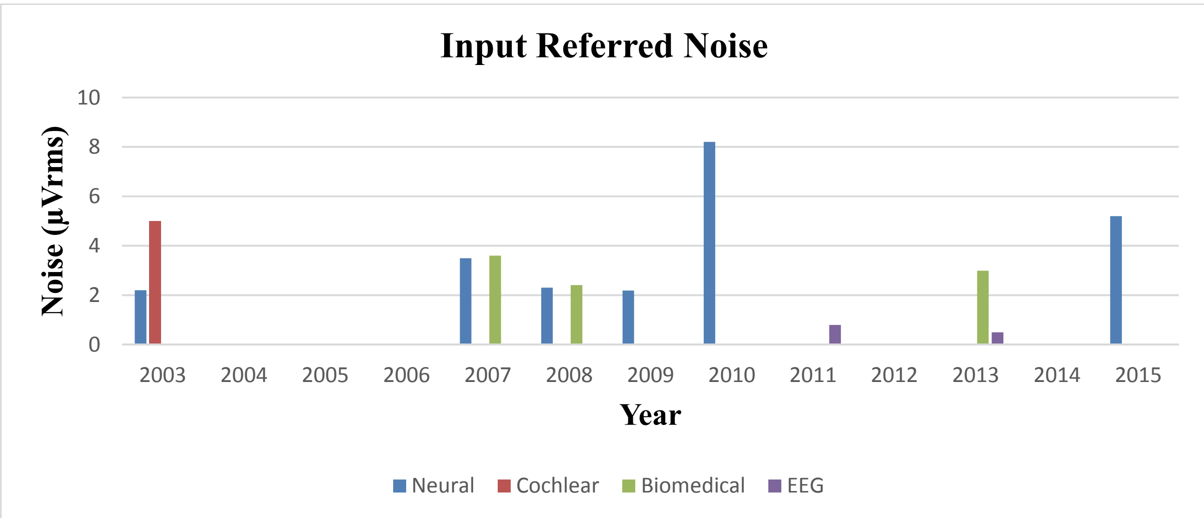

Fig. 15: Input Referred Noise performance trend for various biomedical applications.

Table 1: Performance comparison of some recently reported low power preamplifiers

Paper	Application	Technique used	Input Amplitude	Input frequency	Power Supply (V)	Gain (dB)	Band width	CMRR (dB)	PSRR (dB)	Noise (Vrms)	Power (W)
[10]	Nerve Cuff Recording	OTA	50µV-500µV	0.1Hz-10KHz	±2.5	40	14KHz	82	-	290n	1.3m
[28]	Neural Recording application	OTA	50µV-500µV	0.1Hz-10KHz	±2.5	-	7.2KHz	≥85	≥83	2.2µ	80µ
[29]	QRS detection	Pseudo differential preamplifier	-	-	1.0-1.8	59	8Hz-30Hz	82	-	-	-
[30]	Neural applications	OTA with CMFB	50µV-500µV	0.1Hz-10KHz	3	39.9	0.1-20KHz	-	-	2.3µ	30µ
[9]	ECG	Two stage Instrumentation amplifier	5µV-5mV	0.05Hz-250Hz	-	45.3	290Hz	90	-	8.1µ	2.8µ
[16]	Neural Recording application	True Logarithmic Amplifier	50µV-500µV	0.1Hz-10KHz	1.2	64.6	0.1Hz-20KHz	-	-	6.7µ	11µ
[31]	Biomedical (EEG,ECG,PCG)	PMOS instrumentation amplifier	-	-	1.8	84.2	-	125	125.3	-	61.5043µ
[19]	DBS	FCSOTA	-	-	2.8	39.4	0.36Hz - 1.3KHz	66	80	3.07µ	2.4µ
[7]	EEG	Chopped Logarithmic amplifier(CPLGA)	0.5µV-100µV	0.5Hz-40Hz	1.8	40	-	253	235	500n	99µ
[32]	Biomedical (EEG,ECG,PCG)	OTA with folded cascode	2.5mVpp	-	1V	67.81	-	104.95	-	9µv/√Hz	7.24µ

The graphical analysis shows that previously the gain from 30 dB has increased to a maximum of 84.2dB for the biomedical applications and the power consumption of as low as 2.4 µW has been achieved .The CMRR trend shows the improvement from 50dB to 253dB.The input referred noise has reduced to around 2.2µVrms from a maximum of 8.1µVrms. The various bio-amplifiers are compared on basis on performance related parameters like gain, Power consumption, CMRR, noise, etc. and the comparison is provided in Table 1.

Conclusion

This paper presents a review of various preamplifier topologies for different biomedical applications. The comparison is done based upon some performance parameters like gain, power, CMRR, PSRR, Noise. The amplitude and frequency ranges for various applications are also evident from the comparison table. Here various methods have been employed to reduce the power consumption and minimize effects of flicker noise that is dominant at low frequencies. Thus future work will consider further optimization to ultra low power level. Also different applications like retinal prostheses, DBS can be considered since much of the work is done on neural implantable devices. Further improvement in gain, CMRR with a new technique can also be considered but with an optimized design trade-off between various parameters.

References

[1] W. Khan, E. Muntimadugu, M. Jaffe, and A. J. Domb, "Implantable medical devices," in *Focal Controlled Drug Delivery*, ed: Springer, 2014, pp. 33-59.

[2] R. J. Baker, *CMOS: circuit design, layout, and simulation* vol. 1: John Wiley & Sons, 2008.

[3] F. Moulahcene, N.-E. Bouguechal, and Y. Belhadji, "A low power low noise chopper-stabilized two-stage operational amplifier for portable bio-potential acquisition systems using 90 nm technology," *International Journal of Hybrid Information Technology,* vol. 7, pp. 16-19, 2014.

[4] F. Silveira and D. Flandre, *Low power analog CMOS for cardiac pacemakers: Design and Optimization in Bulk and SOI Technologies*: Springer Science & Business Media, 2004.

[5] S. Ahmed and V. Kakkar, "Modeling and simulation of an eight-bit auto-configurable successive approximation register analog-to-digital converter for cardiac and neural implants," *SIMULATION,* p. 0037549717716537, 2017.

[6] S. Ahmed, S. Bashir, B. Bilal, and V. Kakkar, "Feasibility of Successive Approximation Register ADC in Ultra Low Power Biomedical Applications," *International Journal of Engineering and Technology,* vol. 9, pp. 338-347, 2017.

[7] R. Chebli and M. Sawan, "Low noise and high CMRR front-end amplifier dedicated to portable EEG acquisition system," in *Engineering in Medicine and Biology Society (EMBC), 2013 35th Annual International Conference of the IEEE*, 2013, pp. 2523-2526.

[8] S. Kumaravel, K. Tirumala, B. Venkataramani, and R. Raja, "A power efficient low noise preamplifier for biomedical applications," *Journal of Low Power Electronics,* vol. 9, pp. 501-509, 2013.

[9] J. D. Bronzino, *Biomedical engineering handbook* vol. 2: CRC press, 1999.

[10] R. Rieger, J. Taylor, and N. Donaldson, "Low noise preamplifier design for nerve cuff electrode recording systems," in *Circuits and Systems, 2002. ISCAS 2002. IEEE International Symposium on*, 2002, pp. V-V.

[11] J. H. Nielsen and E. Bruun, "A CMOS low-noise instrumentation amplifier using chopper modulation," *Analog Integrated Circuits and Signal Processing,* vol. 42, pp. 65-76, 2004.

[12] Y. Masui, T. Yoshida, T. Mashimo, M. Sasaki, and A. Iwata, "A 1V Supply Low Noise CMOS Amplifier Using Noise Reduction Technique of Autozeroing and Chopper Stabilization," *IEICE Transactions on Electronics,* pp. 769-774, 2006.

[13] M.-Z. Li and K.-T. Tang, "A low-noise low-power amplifier for implantable device for neural signal acquisition," in *Engineering in Medicine and Biology Society, 2009. EMBC 2009. Annual International Conference of the IEEE*, 2009, pp. 3806-3809.

[14] J. Holleman and B. Otis, "A sub-microwatt low-noise amplifier for neural recording," in *Engineering in Medicine and Biology Society, 2007. EMBS 2007. 29th Annual International Conference of the IEEE*, 2007, pp. 3930-3933.

[15] S.-I. Chang and E. Yoon, "A 1µW 85nV/√ Hz pseudo open-loop preamplifier with programmable band-pass filter for neural interface system," in *Engineering in Medicine and Biology Society, 2009. EMBC 2009. Annual International Conference of the IEEE*, 2009, pp. 1631-1634.

[16] Z. H. Derafshi and J. Frounchi, "Low-noise low-power true logarithmic amplifier for neural recording applications," in *Biomedical Engineering and Sciences (IECBES), 2010 IEEE EMBS Conference on*, 2010, pp. 381-384.

[17] S. Dwivedi and A. Gogoi, "Local field potential measurement with low-power area-efficient neural recording amplifier," in *Signal Processing, Informatics, Communication and Energy Systems (SPICES), 2015 IEEE International Conference on*, 2015, pp. 1-5.

[18] J. Tripathi, R. S. Tomar, and S. Akashe, "Neural signal front-end amplifier in 45 nm technology," in *Communication Networks (ICCN), 2015 International Conference on*, 2015, pp. 223-227.

[19] C. Qian, J. Parramon, and E. Sanchez-Sinencio, "A micropower low-noise neural recording front-end circuit for epileptic seizure detection," *IEEE Journal of Solid-State Circuits,* vol. 46, pp. 1392-1405, 2011.

[20] C.-C. Huang, S.-H. Hung, J.-F. Chung, L.-D. Van, and C.-T. Lin, "Front-end amplifier of low-noise and tunable BW/gain for portable biomedical signal acquisition," in *Circuits and Systems, 2008. ISCAS 2008. IEEE International Symposium on*, 2008, pp. 2717-2720.

[21] J. T. Li, S. H. Pun, P. U. Mak, and M. I. Vai, "Analysis of op-amp power-supply current sensing current-mode instrumentation amplifier for biosignal acquisition system," in *Engineering in Medicine and Biology Society, 2008. EMBS 2008. 30th Annual International Conference of the IEEE*, 2008, pp. 2295-2298.

[22] W. A. Serdijn, A. C. Van Der Woerd, J. Davidse, and A. H. van Roermund, "A low-voltage low-power fully-integratable front-end for hearing instruments," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications,* vol. 42, pp. 920-932, 1995.

[23] M. W. Baker and R. Sarpeshkar, "A low-power high-PSRR current-mode microphone preamplifier," *IEEE Journal of Solid-State Circuits,* vol. 38, pp. 1671-1678, 2003.

[24] V. Kakkar, S. Ahmed, and S. Koul, "An Enhanced Pre-Amplifeir for Cochlear Implants," *Acta Technica Napocensis: Electronica Telecomunicatii,* vol. 56, pp. 13-17, 2015.

[25] M. J. Burke and D. T. Gleeson, "A micropower dry-electrode ECG preamplifier," *IEEE Transactions on Biomedical Engineering,* vol. 47, pp. 155-162, 2000.

[26] A. Gerosa, A. Maniero, and A. Neviani, "A fully integrated two-channel A/D interface for the acquisition of cardiac signals in implantable pacemakers," *IEEE Journal of Solid-State Circuits,* vol. 39, pp. 1083-1093, 2004.

[27] L. Fay, V. Misra, and R. Sarpeshkar, "A micropower electrocardiogram amplifier," *IEEE transactions on biomedical circuits and systems,* vol. 3, pp. 312-320, 2009.

[28] R. R. Harrison and C. Charles, "A low-power low-noise CMOS amplifier for neural recording applications," *IEEE Journal of solid-state circuits,* vol. 38, pp. 958-965, 2003.

[29] K. Lasanen and J. Kostamovaara, "A 1-V analog CMOS front-end for detecting QRS complexes in a cardiac signal," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 52, pp. 2584-2594, 2005.

[30] M. H. Zarifi, J. Frounchi, S. Farshchi, and J. Judy, "A low-power, low-noise neural-signal amplifier circuit in 90-nm CMOS," in *Engineering in Medicine and Biology Society, 2008. EMBS 2008. 30th Annual International Conference of the IEEE*, 2008, pp. 2389-2392.

[31] H.-C. Chow, B.-S. Tang, J.-H. Tien, and W.-S. Feng, "A high performance current-mode instrumentation amplifier for biomedical applications," in *Signal Processing Systems (ICSPS), 2010 2nd International Conference on*, 2010, pp. V2-64-V2-67.

[32] H. S. Raghav, B. Singh, and S. Maheshwari, "Design of low voltage OTA for bio-medical application," in *Emerging Research Areas and 2013 International Conference on Microelectronics, Communications and Renewable Energy (AICERA/ICMiCR), 2013 Annual International Conference on*, 2013, pp. 1-5.