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Numerical simulation and comparative assessment of DG-HEMT device for high-frequency application

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Abstract:

The main objective of this paper is to perform the DC and AC performances of GaN/InGaN/GaN Double Gate High Electron Mobility Transistor (DG-HEMT) based on innovative materials III-V in particular III-N materials (Nitride Materials) by using SILVACO TCAD device simulator. First, we modelled the structure with optimized physical and geometrical parameters. Secondly, we investigated the DC and AC performances; the device offers a maximum drain current of 1.6 A/mm, a threshold voltage of -2.2 V, a maximum transconductance of 0.8 S mm^{-1}, a Ion/Ioff ration of 10^{10}, a Drain Induced Barrier Lowering (DIBL) of 37 mV/V, a Sub-threshold Swing (SS) of 75 mV/dec and a Gate-leakage of 1.10^{-12} A. In terms of AC performances, the device exhibits a cut-off frequency (Ft) of 990 GHz and a maximum oscillation frequency (Fmax) of 2 THz. Finally, a comparison study was carried out with a recent state of the art.

Keywords: GaN, InGaN, AlGaN, DG-HEMT, DC performances, AC performances.

1. Introduction:

The III-V materials are promising and attractive compound semiconductors to develop high power with high frequency and very large scale integration circuits for next generation of RF applications such as high power amplifiers for space research, remote sensing, imaging systems and low noise wide bandwidth amplifiers design [1]. The high performances of recent electronic circuits are highly recommended for recent technology advances in digital and analog systems [2]. A dramatic performance in terms of frequency has been achieved [3-4]. In fact; III-V materials in particular III-N materials have a wide band gap energy and can potentially support a high breakdown voltage, also a high electron mobility serves to lead these components in the future to operate in high speed and low power computing [5].

The high electron mobility transistor based on III-V materials is a suitable device for terahertz frequency range [6] and the scaling down of the device's dimensions in order to minimize the transit time of careers and enhancing electrostatic integrity in the channel [7-8].

Scaling down the device's dimensions resulting an ultra short gate length; due to that, the device faces a severe undesirable effect such as short channel effect (SCE's) [8]. This effect heavily affects the DC and AC performances [9]. An appropriate parameter which is the aspect ratio needs to be maintained to minimize or suppress the short channel effect (SCE's) [10]. The aspect ratio represents the ratio of gate length and the distance from the gate electrode to the channel in the vertical direction [11].

The development of the technology leads to the use of double gate structure and the purpose is to mitigate the undesirable effects such as short channel affects (SCEs) so that can play a significant role to suppress the harmful effects on DC and AC performances [12-13]. The DG structure features of two gates electrodes deposited on the top and back sides; this architect structure provides an excellent electrostatic control of the device. Also; it contains two donor layers which serve to provide free electrons to the channel which improves the current density in the channel, another advantage is no buffer layer in this structure which means no substrate carrier injection. This results a dramatic enhancement of the performances and a better charge control of the device [14].

Our work consists to investigate the DC and AC performances of a DG-HEMT based on nitride materials, and to make a comparison with DG-HEMTs based on III-V materials obtained in state-of-the-art to demonstrate the importance of using innovative materials such as nitride alloys in these devices in microwave applications. It is organized according to the following parts: in the first section, the aim of our work is introduced. A second section is dedicated for the presentation of the simulated structure and different simulation models such as physical models and numerical method used also different physical and geometrical parameters. The third section contains the simulated DC and AC characteristics. Furthermore, a comparison study is carried out in order to validate our results and prove the importance of developing research through the use of III-V materials in particular III-N materials in these devices for high frequency and high power applications. Finally, a general conclusion is presented. The device performances are performed by using numerical simulation tools (SILVACO TCAD).

2. Device structure and simulation models

The schematic cross section of the simulated structure is shown in the Fig. 1. The device features the following physical and geometrical parameters: an undoped Schottky layer of $Al_{0.25}Ga_{0.75}N$ and 1 nm of thick, a donor layer of $Al_{0.25}Ga_{0.75}N$ with n-doping concentration of 3e19 cm^{-3} and a thickness of 7 nm. An undoped spacer layer of GaN with 1 nm of thick is inserted between the donor and channel layers to separate the ionized donor atoms and the free electrons of the channel layer which furthermore improves the channel mobility; the channel layer is an undoped $In_{0.75}Ga_{0.25}N$ with 10 nm of thickness.

The layers below the channel are identical to the one above the channel in order to form DG-HEMT structure. The gate length is fixed to 15 nm and the area of the device is 0.5 µm × 200 µm. The gate-source spacing (L_{GS}) and the gate-drain spacing (L_{GD}) are fixed to 110 nm and 370 nm, respectively. The table 1 shows the meaning of structure parameters.

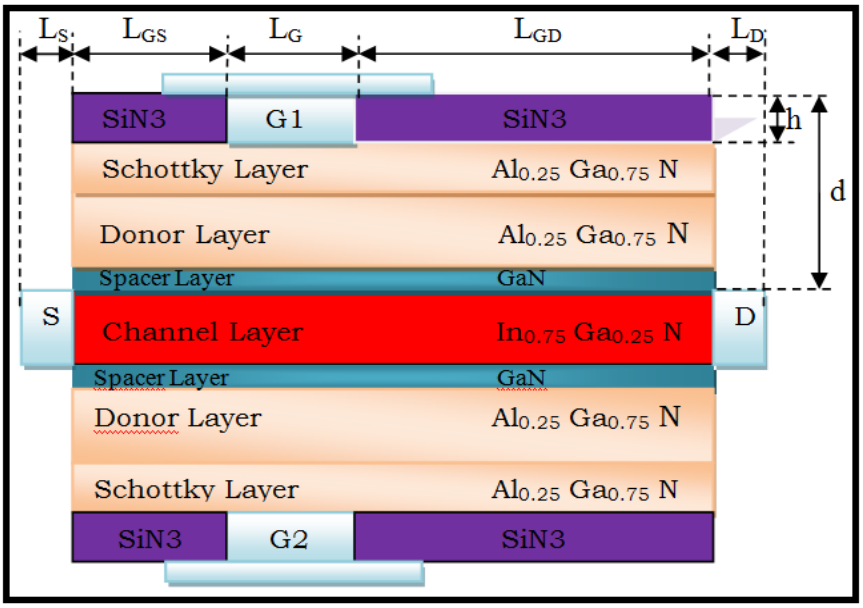

Fig. 1: Schematic cross section of the simulated DG-HEMT.

Table. 1: Meaning of structure parameters.

Structure parameters	Value (nm)
Gate length (L_G)	15
Spacing between gate to source side (L_{GS})	110
Spacing between gate to drain side(L_{GD})	370
Drain length in x direction (L_D)	10
Source length in x direction (L_S)	10
Thickness of SiN passivation layer (h)	10
Spacing between drain and top side (d)	19

The simulation is performed in 2D with GUMMEL-NEWTON as numerical method to resolve Poisson and continuity equations. Taken from Silvaco ATLAS user's manuals [15], the physical models included in the simulation are the Shockley-Read-Hall (SRH) recombination mechanism to account the recombination effects, AUGER recombination to take accounts the high level injection effects, Bandgap Narrowing (BGN), and Parallel Electric Field (FLDMOB) to model the velocity saturation effect.

The physical parameters of the binary materials, GaN, AlN and InN are taken from Silvaco Atlas user's manual [15-16]; and the physical parameters of the ternary materials,

$In_{0.75}Ga_{0.25}N$ and $Al_{0.25}Ga_{0.75}N$, are deduced by linear interpolation according to the Vegard law [17].

3. Results and discussion

DC performances

The Fig. 2 shows the energy band diagram, it presents the conduction and valence band energies as a function of depth from surface along the vertical direction of the device GaN/$In_{0.75}Ga_{0.25}N$/GaN.

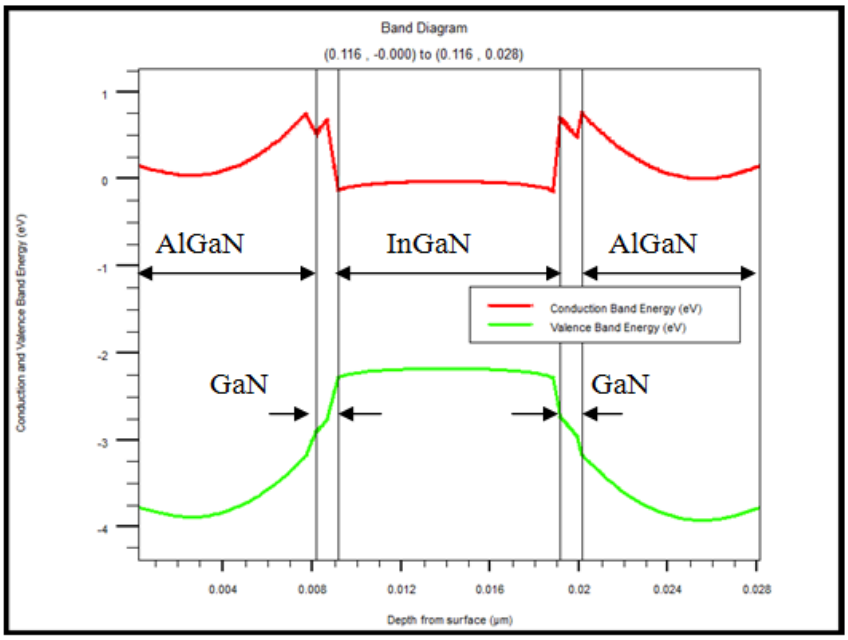

Fig. 2: Energy band diagram of DG-HEMT.

Fig. 3 shows the output characteristics: the drain-source current (Ids) as a function of drain-source voltage (Vds) for different gate-source voltages. The drain-source bias is swept from 0 V up to 5.0 V while the gate-source voltage is swept from 0 V to - 2.2 V. The maximum drain current obtained is 1.6A/mm at Vgs = 0.0V. This high saturated drain current is obtained with undoped channel and 10 nm of thickness, due to high electron density in the channel, and a knee voltage (Vknee) only of 0.5 V.

Fig. 4 shows the transfer characteristics: the drain-source current (Ids) as a function of gate-source voltage (Vgs) while the drain voltage is fixed at 1.0 V and 5.0 V, and the gate-source voltage was swept from 0.0 V to -3.3 V. The device presents a low threshold voltage due to an excellent control of the channel. The threshold voltages were about -2.1 V and -2.25 V for drain-source voltages (Vds) of 1.0 V and 5.0 V, respectively.

Fig. 5 shows the transconductance (gm) as a function of gate-source voltage (Vgs). The transconductance is the expression of the control mechamism of field effect transistors. Heterojunction Field Effect Transistors (HFETs) are characterized from all other FETs

devices by their high transconductance. The simulated device exhibits a maximum transconductance of 800 mS/mm at -1.0 V gate-source voltage while drain-source voltage is fixed at 1.0 V.

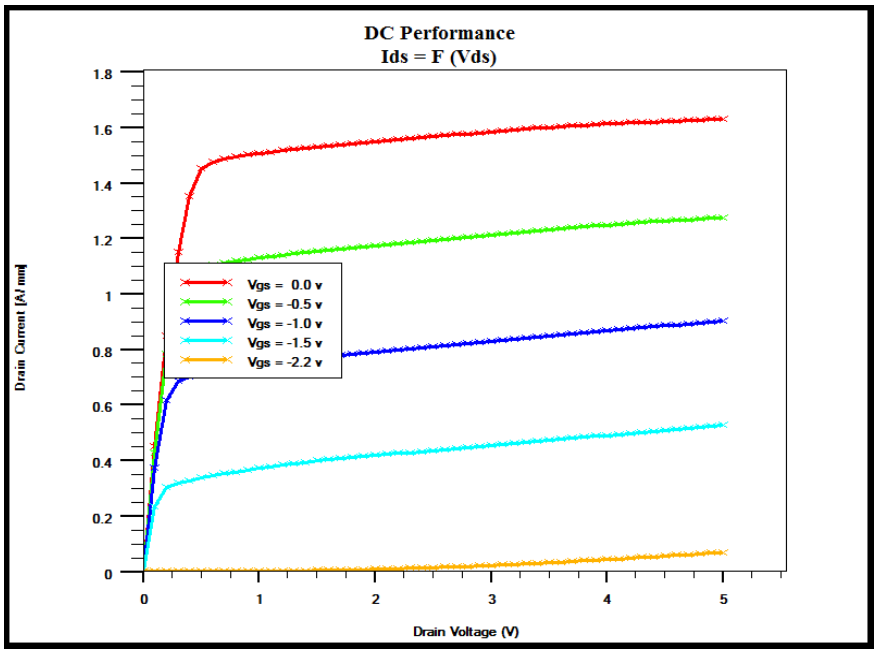

Fig. 3: The drain-source current as a function of drain source voltage while Vgs is swept from 0.0 V to -2.2 V, and Vds from 0.0 V to 5.0 V.

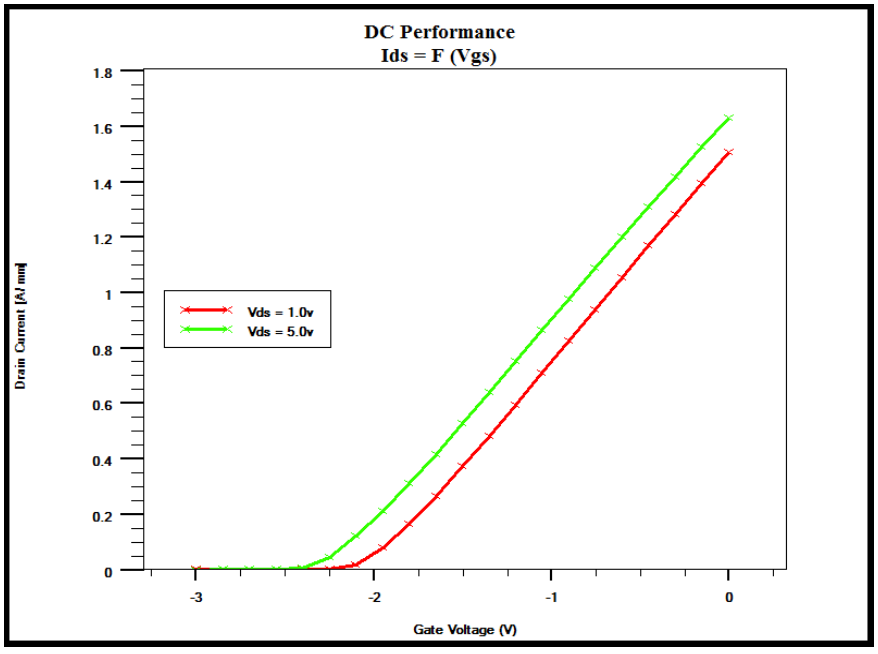

Fig. 4: The drain-source current (Ids) as a function of gate-source voltage (Vgs) while drain voltage is fixed at 1.0 V and 5.0 V, and gate-source voltage is swept from 0 V to -3.3 V.

The Drain Induced Barrier Lowering (DIBL) is an important parameter describing electrostatic integrity of The High Electron Mobility Transistor (HEMT). It is defined as the ratio of threshold voltage (V_{th}) change to the drain-source voltage (Vds) change (ΔV_{th} / ΔV_{ds}) [28]. In this work the DIBL is calculated at the difference between V_{th} for V_{ds1}=1.0v and V_{ds2}=5.0v. The DIBL is calculated by the equation (1).

$$\text{DIBL} = \text{abs}\left[\frac{\Delta \text{Vth}}{\Delta \text{Vds}}\right] = abs\left[\frac{Vth2-Vth1}{Vds2-Vds1}\right] \quad (1)$$

$$\text{DIBL} = abs\left[\frac{-2.25-(-2.1)}{5-1}\right] = \text{abs}\left[\frac{-0.15}{4}\right] = 0.037\ V/V$$

DIBL = 37 mV/V

Where V_{th1} = -2.1v at Vds = 1.0v and V_{th2} = -2.25v at Vds = 5.0v

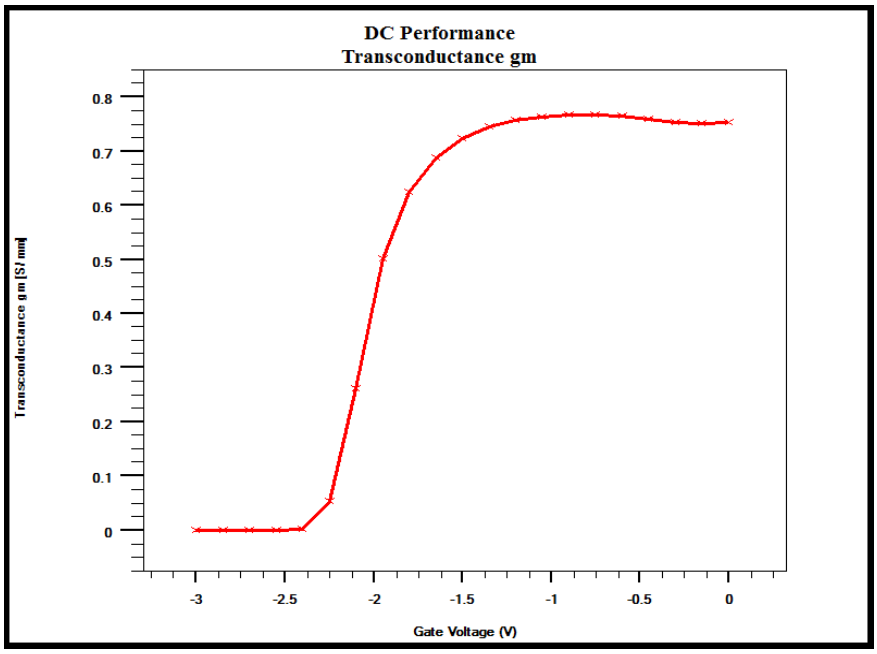

Fig. 5: Transconductance versus the gate-source voltage while drain-source bias is fixed at 1.0 V.

Fig. 6 shows the gate-leakage current as a function of gate-source voltage, while the drain bias is fixed at 1.0 V and the gate source is swept from 1.0 V to - 3.0 V for a DG-HEMT device based on nitride materials. The gate-leakage current is invariant with the gate bias, the device offers a gate leakage only of 1.10^{-12} A at -3.0 V gate bias. This extremely low value is evident to indicate the high quality of the device.

Fig. 7 shows the drain-source current plotted with log scale as a function of gate-source voltage. The On-state indicates the saturation current while the Off-state current is the sum of

total leakage current which includes sub-threshold, gate and junction leakage current [18]. The Ion/Ioff ratio extracted from the characteristics is about 10^{10}. A high value of Ion/Ioff ratio is crucial parameter for power application. Furthermore, this parameter has an attractive attention on power consumption in static and standby power applications.

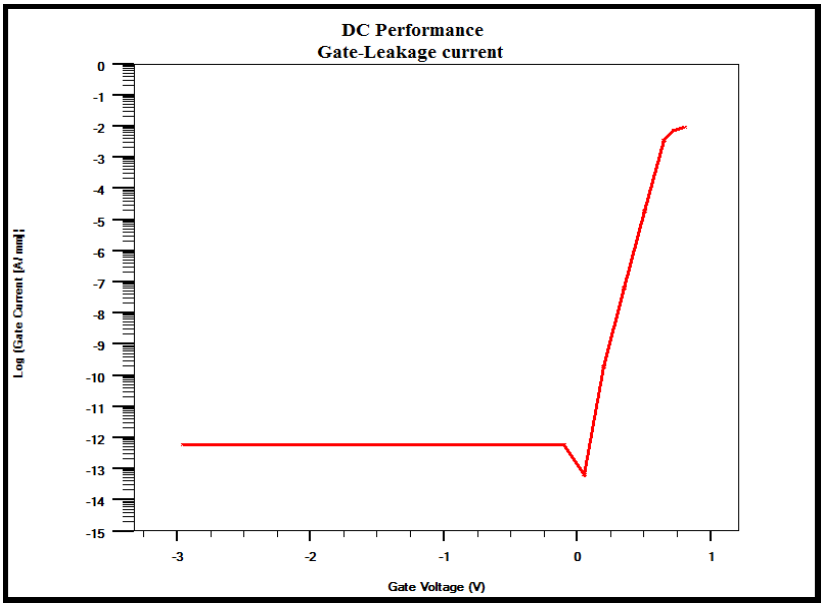

Fig. 6: Gate-leakage current as a function of gate-source voltage.

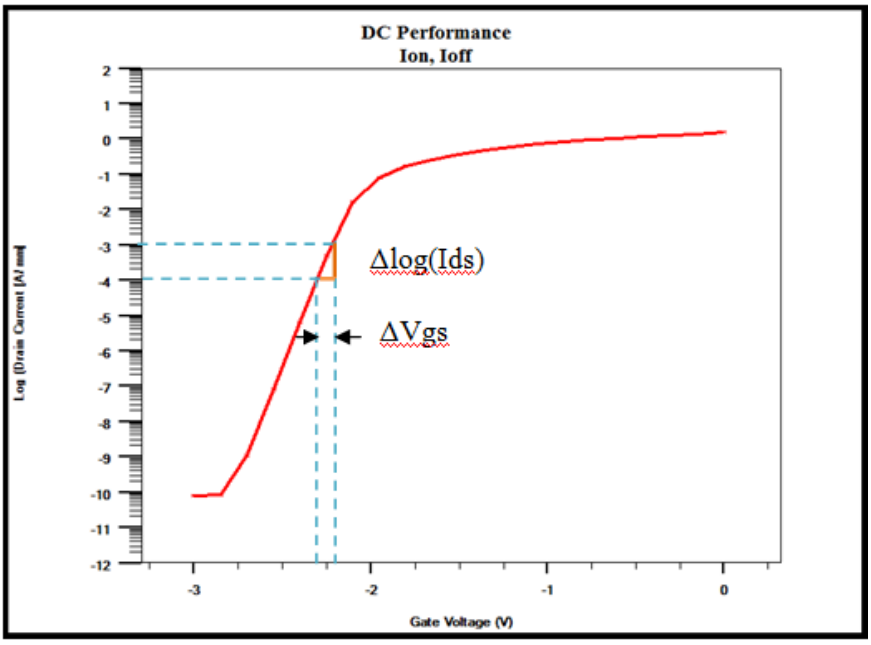

Fig. 7: Drain current plotted with log scale as a function of gate-source voltage.

The Sub-threshold Swing (SS) is determined on the log (Ids) characteristic as a function of Vgs. It corresponds to the gate-source voltage to be applied to reduce the drain current by one decade. it is defined in mV / dec. The SS is calculated by the equation (2).

Sub-threshold slope $\Longrightarrow SS = \frac{\Delta Vgs}{\Delta \log(Ids)}$ (2)

$$SS = \Delta Vgs/dec$$
$$SS = Vgs2 - Vgs1/dec$$
$$SS = [-2.2125 - (-2.1375)]\, V/dec$$
$$SS = 0.075\, V/dec$$
$$SS = 75\, mV/dec$$

AC performance

In this part, we perform the AC performances of the device by analyzing two important parameters: the cut-off frequency (ft) and the maximum oscillation frequency (fmax) [19]. The ft and fmax are evaluated when the current gain and the power unilateral gain are unities [20-21].

Fig. 8 shows the current gain and unilateral power gain as a function of the frequency, while the drain bias is fixed at 1.0 V and the gate bias is fixed at 0.0 V.

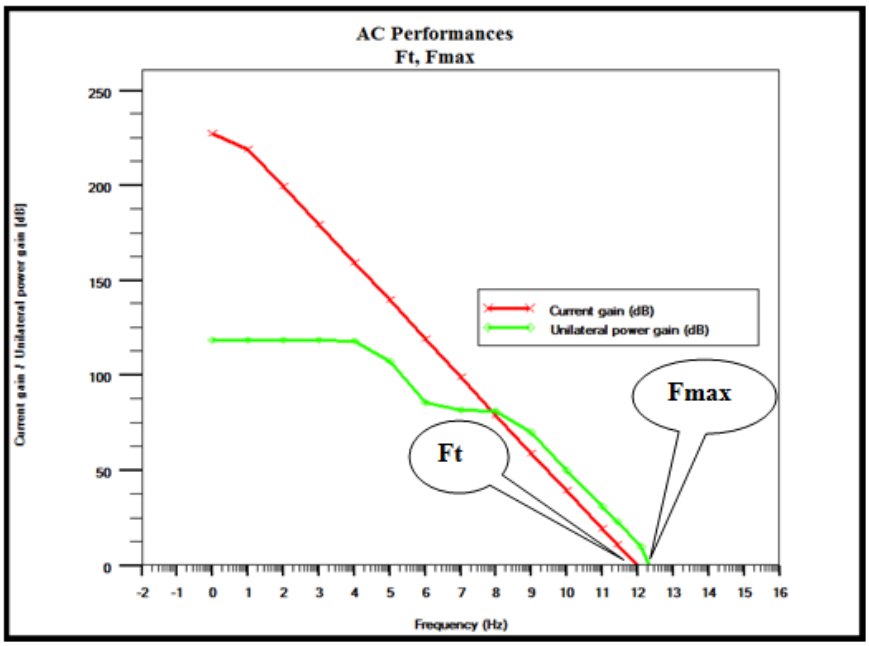

Fig. 8: The current gain and the unilateral power gain as a function of the frequency, while the drain bias is fixed at 1.0 V, and the gate bias is fixed at 0.0 V.

For a gate length of 15 nm, the device exhibits a cut-off frequency of 990 GHz and a maximum oscillation frequency of 2 THz, while the drain-source voltage is fixed at 1.0 V. The device exhibits excellent AC performances compared to the results found in the state of the art.

The results found are very impressive and attractive for power applications and terahertz range; the reason is the use of particular nitride materials, and the source and drain electrodes

are in direct contact with the channel layer. In a conventional structure, these electrodes are far from the channel layer, and would give lower RF performance.

The table 2 contains the device's characteristics and the table 3 and 4 presents a comparison of our results such as the cut-off frequency (Ft) , the maximum oscillation frequency (Fmax) and digital characteristics with the highest values reported in the state of the art.

Table 2: Device characteristic of the simulated DG-HEMT.

Device's characteristics of DG-HEMT with gate length of 15nm	**Results**
Drain current I_D (A/mm)	1.6
Threshold voltage Vth (V)	-2.2
Transconductance gm (S/mm)	0.8
Drain Induced Barrier Lowring DIBL (mV/V)	37
Sub-threshold Swing SS (mV/dec)	75
Gate-leakage current (A)	1.10^{-12}
Ion/Ioff ratio	1.10^{10}
Cut-off frequency Ft (Ghz)	990
Maximum oscillation frequency Fmax (Ghz)	2000

Table 3: Comparison of highest reported Ft and Fmax in the state of the art based on III-V

materials with our reported DG-HEMT based on III-N materials (Nitride materials).

Reference	**Gate length (nm)**	**Ft (Ghz)**	**Fmax (Ghz)**	**Year**
[22]	100	192	288	2004
[23]	100	-	257	2006
[24]	50-100	258-214	286-287	2007
[25]	50	175	448	2013

[26]	30	776	905	2017
[27]	30-50	825-710	1082-989	2017
[8]	30	809	1030	2018
This work	**15**	**990**	**2000**	**2018**

Table 4: Comparison of highest reported DC performances in the state of the art based on III-V materials with our reported DG-HEMT based on III-N materials (Nitride materials).

Reference	L_G (nm)	I_D (A/mm)	V_{th} (V)	Gate-leakage (A)	gm (S/mm)	I_{on}/I_{off}	DIBL	SS	Year
[22]	100	0.6	-0.4	-	2.8	-	-	-	2004
[23]	100	0.82		-	2.3	-	-	-	2006
[24]	100	0.56	-0.4	-	2.6	-	15	75	2007
[25]	50	-	-	-	1.81	-	-	-	2013
[26]	30	0.98	0.29	-	3.09	$2.24x10^5$	68	73	2017
[27]	50	1.42	0.26	-	3.58	-	58	62	2017
[8]	30	1.2	0.21	-	3.3	-	-	-	2018
This work	**15**	**1.6**	**-2.1**	**1.10^{-12}**	**0.8**	**1.10^{10}**	**37**	**75**	**2018**

Conclusion:

In summary, we have investigated the DC and AC performances of a DG-HEMT based on III-V materials in particular nitride materials (III-N) by using two dimensional TCAD simulator (SILVACO TCAD). The use of two gates on both sides of the device provides a

significant improve in its performances which become very dominant in high power and high field conditions. The better channel control with double gate (DG) has been achieved by suppressing the undesirable effect such as short channel effect (SCE) in terms of DIBL and SS. The device exhibits a maximum drain current of 1.6 A/mm, a threshold voltage of -2.2 V, a maximum transconductance of 800 mS mm^{-1}, an Ion/Ioff ratio of 10^{-10}, a Drain Induced Barrier Lowering (DIBL) of 37 mV/V, a Sub-threshold Swing (SS) of 75 mV/dec, and a Gate-leakage current of 1.10^{-12} A. Furthermore, a dramatic AC performance in terms of cut-off frequency (Ft) and maximum oscillation frequency (Fmax) has been achieved. A comparison study was carried out with a recent state of the art and the obtained results provide a reference for future research to use III-V materials in particular nitride materials (III-N) for power applications and terahertz range.

Acknowledgments

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