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Analysis of Reducing Total Harmonic Distortion in a PV integrated Micro Inverter

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ABSTRACT

The significant growth in photovoltaic (PV) energy is experienced in the last decade because of price reduction of PV modules and the revolution of PV micro inverters. High performance and reliability are the key merit to match the life time of PV and micro inverter. Multilevel micro inverters are mostly used for DC to AC power conversion, and they are divided into two types: current source inverters (CSI) and voltage source inverters (VSI). In the power industry, voltage source micro inverters are much more commonly used to convert lower DC voltages to higher AC voltages. The frequently used pulse width modulated (PWM) switching technology of DC sources introduces harmonics into the inverter output voltage during conversion. Total harmonic distortion (THD) is a measure of harmonic pollution in the power system, and it has been discovered that THD of inverter output voltage is affected by fluctuations in both DC voltages and switching angles of inverters. This study covers inverters with unequal DC sources, which is a reasonable and practical assumption. Evolutionary analysis is used to find the best DC voltages and switching angles for minimizing THD. This paper proposed a reliability and performance enhancement of micro inverter and new design has been proposed in single level and cascaded multilevel micro inverter for full irradiance and partial shading conditions. Design analysis with mathematical modeling is presented for the analysis of voltage and current ripples as well as for total harmonic distortion (THD). Two different scenarios are presented for simulations using MATLAB as tool. Results reveal that partial shading does increase the 44.01 % harmonics with cascaded inverters; however, the impact is limited as compared to single level micro inverter.

Keywords: Micro inverter, reliability, performance, photovoltaic

1. INTRODUCTION

In previous last few decades, it is observed that the demand of renewable energy systems increased constantly due to the consumption of fossil fuels globally and the contribution of solar PV is much more than other renewable sources. For the production of solar energy, PV inverter is essential which transfer PV energy to load or grid [1]. The inverters which connected the grid to PV are classified in central inverters, string inverters and AC module inverters which is also known as micro inverter. A multilevel voltage source inverter is a power electrical device used in high voltage, high power

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applications in the current day. The inverter's major design topologies are diode-clamped, flying capacitor, and cascaded H-bridges. PWM switching is used most of the time. While this method of producing AC is reliable, the output voltage is not entirely sinusoidal, resulting in harmonics in the output voltage. The output voltage approaches the sine wave as the number of voltage steps in the inverter increases. Due to hardware limitations, however, the levels can only be extended to a certain point. The harmonic content of the inverter output is impacted by switching instances of various voltage sources. With proper switching angle selection, THD can be reduced to a minimum. To identify appropriate switching angles, iterative algorithms and soft computing methods might be used. SHE (selective harmonic elimination) is a strategy for reducing harmonic content even more. This method considers the idea that lower order harmonics are the more prevalent in the system; therefore, eliminating them will significantly reduce overall THD levels. Inverters with equal DC sources are obviously easier to model mathematically than micro inverters having unequal DC sources [2].

In technical literatures, the PSO, real coded GA, and Bee algorithms are used to solve transcendental equations to provide switching angles for harmonic elimination of inverter with unequal DC sources. However, in their research, predefined values of asymmetrical DC sources are used, and optimization simply yields switching angles [3]. The goal of this study is to reduce the THD of a cascaded H-bridge multilevel inverter by optimizing both DC source voltages and switching angles without removing any specific harmonic order. Furthermore, the phase THD is calculated using an exact formula [4], which does not impose any restrictions on harmonic order consideration. Accounting harmonics up to a finite order in THD calculations, such as up to the 49th, 63rd, 97th, or 199th harmonic, frequently results in an error that can be considerable in higher level inverters [6]. The algorithm employed in this paper calculates precise phase THD by finding a set of ideal DC voltages and switching angles for various levels of inverters [5].

For medium or high voltage and other applications, multilevel inverters are commonly employed [6]. Many recent multilevel inverter publications end up with voltage THD assessment conclusions that are often based on numerical calculations or measurements of voltage frequency spectra. To measure multilevel voltage quality, a portion of the multilevel research community adopts a limited harmonics count (49 as indicated by IEEE Standard 519 [7] or another number like 101). First, this results in voltage THD underestimate, which is notably noticeable for reasonably high frequency PWM (an inaccuracy of up to 100% is possible). Second, THD of line (line-to-line) voltage and phase (line-to-neutral) voltage differ in a practical scenario of a three phase inverter with a star-connected balanced load with just an isolated neutral. Simple time domain and symmetry considerations, on the other hand, indicate that the line and phasing voltage THD are the identical in this situation [8]. A cascaded H-bridge multilevel inverter is defined as a series connection of a number of single phase inverters [9]. By expanding the number of tiers of inverters, the power rating of the inverter can be enhanced without requiring greater ratings of individual devices [11]. A two-level Voltage Source Inverter (VSI) can produce a zero or VDC (two-level) current or voltage output. However, as the name implies, multilevel inverters can create any level of current or voltage. The output voltage of a multilevel inverter is produced in short stages, which determine the inverter's level [12]. Multilevel inverters are divided into three categories: (i) diode clamped multilevel inverters, (ii) flying capacitor multilevel inverters, and (iii) cascaded H-bride multilevel inverters. The cascaded H-bridge inverter topology is particularly popular among electrical engineers because of its simplicity. Each H-bridge in a cascaded H-bridge multilevel inverter has its own DC source. The primary goal of this research is to reduce THD at the output of a cascaded H-bridge multilevel inverter [13]. The power quality can be improved and the THD can be reduced by regulating the switching angle of switches.

1.1 Working of H-Bridge Cascaded Micro Inverter

When a pulse is applied to the gate of a switch, it turns on and stays on until the gate supply is turned on. When the gate supply is cut off, the switch turns off. Figure 1 shows the circuit diagram of a single phase 11-level cascaded H-bridge multilevel inverter. In the diagram, five H-bridges are connected in series to create an 11-level cascaded H-bridge multilevel inverter. Every H-bridge in the cascaded H-bridge has its own DC source.

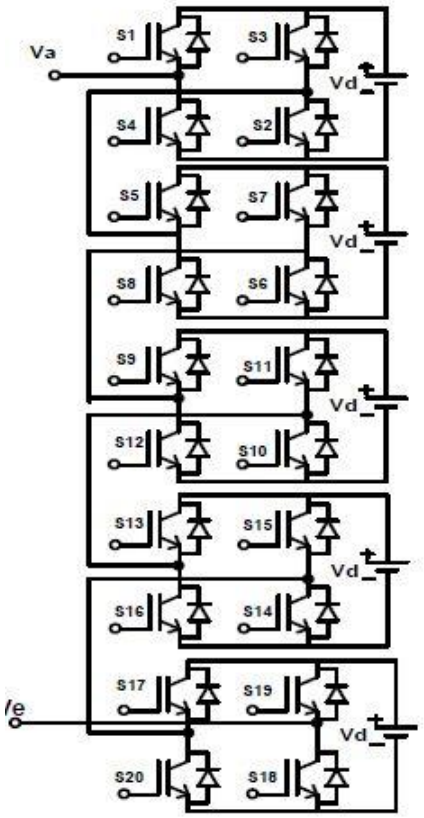

Figure 1. Cascaded multilevel micro inverter

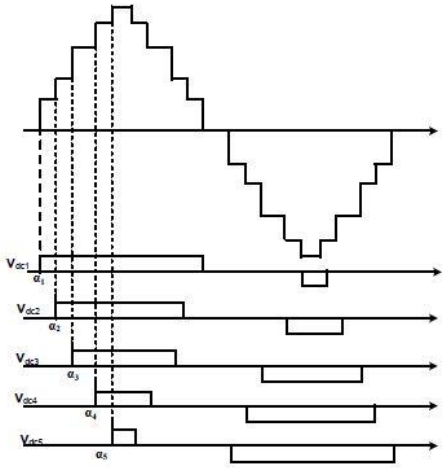

Figure 2. Micro inverter switching pattern

The voltage waveform of a cascaded H-bridge, multilevel inverter with five distinct DC sources is shown in Figure 2. The inverter is switched at the fundamental frequency, and the voltage output waveform is nearly sinusoidal, with a Total Harmonics Distortion of roughly 7.05 % [14].

1.2 Analysis of Total Harmonic Distortion

THD is used to evaluate the quality of a voltage or current waveform. The acquired current or voltage waveform is compared to the basic waveform to determine the THD. When THD is low, two waveforms are said to be identical. The most significant features of an inverter are its efficiency and output power quality, while THD specifies supply power quality. Figure 1 shows the circuit diagram of a single phase 11-level cascaded H-bridge multilevel inverter. In the diagram, five H-bridges are connected in series to create an 11-level cascaded H-bridge multilevel inverter. Every H-bridge in the cascaded H-bridge has its own DC source. THD analysis was carried out on 11-level cascaded H-bridge multilevel inverter at a frequency of 50Hz. The selective harmonics technique was applied on various firing angles to delete specific harmonics, and the 5th, 7th, 11th, and 13th harmonics were eliminated in this case. The THD of an 11-level cascaded H-bridge multilevel inverter was determined to be around 20%, and we may further reduce the THD by increasing the level of the cascaded H-bridge multilevel inverter [14].

Nowadays, PV connected micro inverters are more popular because of its flexibility in expansion, system installation and high level energy harvesting under partial shading conditions. In the last few years, the new schemes of transformer less PV micro inverters are designed which reduced the line frequency transformer cost and achieved and the high efficiency [15]. In less PV micro inverters transformer, it uses the neutral point clamp (NPC) and T-type topologies which are not suitable in low power applications. The expected annual growth of solar PV micro inverter is 15.3% for the year (2016 to 2026) and will reach to the $1969.7 by the end of 2026. The PV inverters are divided into Micro inverters, string inverters and centralized inverters and ranges from few watts to kilowatts [16]. The main drawback of string and centralized inverter is that it does not achieve the maximum power point tracking. Integrated micro inverter with PV has been able to achieve MPPT solution. This paper presents a comprehensive analysis on the reduction of voltage ripples and total harmonic distortion in single level micro inverter [17]. The major advantages and experimental results in this regard will be discussed to find the optimal solution.

Table 1. Critical study of existing research work in the area of micro inverter reliability

Reference	Methodology	Parameters Addressed	Achievements	Deficiencies
Ref [1]	Experimental verification and analysis of Micro inverter topologies.	Efficiency, power density, reliability and cost.	Estimated efficiency and loss breakdown.	high efficiency, high power density, and low cost
Ref [2]	Two-stage high-efficiency micro-inverter system with grid Volt/VAR support functions is designed.	Good switching variation, inverter loss breakdown, efficiency and total system cost.	Various design Trade-offs such as topology, control, filter solutions, and power supplies, and mechanical packaging are provided.	Power density and Reliability.
Ref [3]	Comparative analysis of stresses and levels for accelerated testing of inverters.	Temperature, humidity and voltage bias effect of the inverters.	inconsistent quality of the Inverters and the durability of components leading to greater cost for the photovoltaic plant operator.	Design validation testing using realistic operation, environmental, and connection conditions, including under end-use field conditions with feedback for continuous improvements.
Ref [4]	Based on stress-factor reliability for calculating the mean time between failures (MTBF) of a photovoltaic module-integrated inverter.	Module temperature, Insulation level and efficacy.	The reliability Of six different candidate inverter topologies for a PV-MII, showing the impact of each component on the inverter reliability.	Smaller data set was considered and no focus on operating cost.
Ref [5]	An energetic self-control strategy for design and prototype realization of a plug-in hybrid electrical	State of charge (SOC), temperature, and sign of the current	Validation and improvement in combustion-engine mode CEM ,	Onboard energy control strategy

	vehicle (PHEV), To analyze and optimize the power flux between the different parts.	(charge or discharge current).	electric-vehicle mode EVM, start-and-stop mode SSM.	and cost optimization.
Ref [6]	Commercial and Industrial power semiconductor modules for grid connected micro inverter.	High Power density, installation cost, minimization of leakage current.	Micro inverter system configuration, economic cost, reliability, high efficiency.	Residential applications, Warranties, Converters with SiC diodes.
Ref [7]	Investigation of subpanel level MPP tracking for increasing yield and reduce mismatching losses.	Efficiency, Power decoupling, MPP tracking.	Higher efficiency, loss model of multi input AC module converter.	Control effort, standby losses, hardware cost, sub string mismatch losses.
Ref [8]	Single phase grid connected PV micro inverter with reactive power support capability, constructed by bi-directional buck boost converter.	Grid voltage, peak current envelope, control strategy, efficiency.	High efficiency at unity power factor operation, reactive power supply using control strategy.	No consideration of cost and losses. Installation positions.
Ref [9]	Grid- tied single phase PV Micro inverter utilizing a split coil inductor.	Micro inverter Losses, control actions and measurements.	Reduced devices with increased number of levels, sole DC source without balance capacitor voltage, reduced semiconductor losses. Highly efficient micro inverter.	Losses ignored, high cost is a major factor.
Ref [10]	Impedance source PV micro inverter based on system level electro thermal modeling	Power loss on junction temperature, enclosure temperature, thermal cross coupling effect between components.	Thermal cross coupling effect , prediction of system wear out failure , long term reliability	Identification of weakest link in PV micro inverter, benchmark various design techniques for reliability improvement. Empirical devices may lead to errors due to different operating

				conditions, Installation positions.
Ref [11]	Two stage micro inverter design of a grid connected PV.	Power conversion efficiency, reliability, Power decoupling.	Long term stress analysis, life time prediction and reliability modeling.	Unreliability distributions for different HEMTs, degradation of PV module will slow down the wear out of micro inverters, failure modules are not considered.
Ref [12]	Physics of failure (PoF) based approach to correlate damp heat test for micro inverter reliability assessment.	Efficiency , output current and voltage ,total harmonic distortion	Damp heat , reliability, time to failure	Electrical Losses, No consideration of cost and losses.
Ref [13]	Improvement of reliability of DC link from reliability oriented and conditioning monitoring of DC link modes.	Reliability, failure mechanism , failure modes , life time models	Reliability oriented design approaches and condition monitoring methods are thoroughly presented	Coupling effect among various stressors on the life time of capacitors, noninvasive condition monitoring methods with less realization effort and higher estimation accuracy.
Ref [14]	MPPT controlled hybrid concept for PV Inverters.	Constant power generation, maximum power point tracking, efficiency, thermal loading, reliability.	Efficiency of annual energy yield in MPPT mode, inverter efficiency of power devices.	Selection of power limit, verification of feasibility, effectiveness of proposed control concept.
Ref [15]	Comparison of selected micro inverter in term of components counts, power rating and CAC efficiency	Power rating , MPPT range, power factor , Power density	The merits and drawbacks of main stream product in micro inverter were demonstrated.	Contributing roles of advanced power decoupling circuits and power semiconductor components are not considered.

Ref [16]	Reliability assessments of single phase PV micro inverter considering mission profile and uncertainty.	Life time model, manufacturing process, ambient temperature, solar irritation	Micro inverter installed in one part of the country has a longer life time than the one installed in some other area. Film capacitors have acceptable life time in the active power decoupling methods.	Reliability oriented investigation, limitation on disregarding temperature cycling and loading condition.

2. Proposed System

Single level and multi-level micro inverters are the power electronics devices which are used in power applications. Major topologies that are used in these types of micro inverters are diode clamped, cascaded H- Bridge and flying capacitor type. The output voltage is obtained from mostly pulse width modulation (PWM) which is advance technique of the switching. Although this technique is effective enough but the output is not the pure sinusoidal waveform and thus introduces the harmonics and ripples in the voltage. Switching limitations of the voltage sources affect the harmonics in the output of the system. Reduction of the total harmonic distortion and ripples compensation can be achieved by the selection of proper switching angles. For this purpose, iterative techniques and computing methods are used for finding switching angles. Selective harmonic elimination (SHE) is the method to reduce the system harmonics. The low order harmonics are always dominant in the system therefore its reduction in the priority level will reduce THD in large extent.

The primary focus for the work is to reduce the THD on the micro inverters and ripples compensation. The analysis carried out in this regard involves the voltage fluctuation of the PV modules with micro inverters and the Total Harmonic distortion percentage. Both of this analysis is carried out in MATLAB environment which provides built-in tools for FFT analysis. The analysis was first carried out on a single inverter with multiple solar PV panels attached to it. Then, individual inverter (micro-inverter) for each of the solar panel was attached and results were checked. After that, the cascaded inverter methodology was checked which has been proven out to be one of the most viable methods for reducing harmonics in the system. In the end, a cascaded inverter for 3 solar modules is separately attached and analysis is done.

2.1 Mathematical Modeling of Pulse Width Modulation

The output of the DC voltage is constant in magnitude that uses PWM switching techniques. The purpose of the micro inverter is to carry the output AC and input voltage to control the frequency and magnitude. There are many techniques of the modulation but the basic method is pulse width modulation. In this method the micro inverter uses frequency of triangle which is mostly kept constant.

Figure 3. Switching frequency of triangular waveform

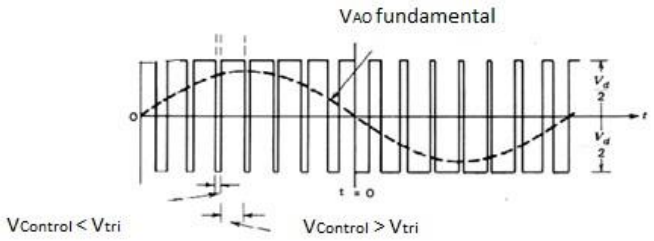

Figure 4. Pulse width modulation (PWM) graph

In Figure 4, pulse width modulation is proportional to the sine-wave amplitude and the gating signals are generated with carrier wave frequency. The modulation index (M) is expressed mathematically as:

$$M = \frac{V_r}{V_c} \qquad (1)$$

where V_r is the peak reference signal magnitude and V_C is the peak carrier signal magnitude. The carrier frequency is dependent on the number of pulses per half cycle. Each pulse responds under the area of sine wave in between the mid points of gating signals. If P_m is the width and the m^{th} is the pulse, then output voltage can be expressed as:

$$V_o = V_{dc}\left(\sum_{m=1}^{Np} \frac{Pm}{\pi}\right)^{1/2} \qquad (2)$$

The pattern used in the switching devices of micro inverters is periodic in nature, therefore its analysis is simple for switching functions by means of Fourier series. For T=1/f, where f is the frequency of the pulses for the time period T and the angular frequency is considered as ω =2πf, and ωT =2π radians, the angular duration for the value period is 2π / A, for value period of zero reference is −π / A, then the Fourier series of that periodic signal is stated as in equation (3):

$$H(\omega t) = \sum_{n=0}^{n=\infty}[C_n \cos(n\omega t) + S_n \sin(n\omega t)] \qquad (3)$$

The coefficient of Fourier expansion can be derived from standard determination of:

$$Sn = \frac{2}{T}\int_{\frac{T}{2}}^{\frac{T}{2}} Hsin(n\omega t)dt$$

$$= \frac{1}{\pi}\int_{\pi/A}^{\pi/A} \sin(n\omega t)\, d\omega t \qquad (4)$$

$$=0$$

$$C_0 = \frac{2}{T}\int_{\frac{T}{2}}^{\frac{T}{2}} H\, dt$$

$$= \frac{1}{2\pi}\int_{\pi}^{\pi} H\, d\omega t \qquad (5)$$

$$= \frac{1}{A}$$

$$C_0(n \neq 0) = \frac{2}{T}\int_{\frac{T}{2}}^{\frac{T}{2}} Hcos(n\omega t)\, dt$$

$$= \frac{1}{2\pi}\int_{\pi/A}^{\pi/A} \cos(n\omega t)\, d\omega t \qquad (6)$$

$$= \frac{2}{\pi}\sin\left(\frac{n\pi}{A}/A\right)$$

Thus,

$$H(\omega t) = \frac{1}{A} + \frac{2}{\pi}\sum_{n=1}^{n=\infty}[\mathrm{Sin}(n\pi/A)/n]\cos\,(n\omega t) \qquad (7)$$

The alternate form for expansion of the average value of 1/A term can be used within the summation:

$$H(\omega t) = \frac{1}{\pi}\sum_{n=-\infty}^{n=\infty}[\mathrm{Sin}(n\pi/A)/n]\cos\,(n\omega t) \qquad (8)$$

Hence, equation 7 can also be written as:

$$H(\omega t) = \frac{1}{A} + \frac{2}{\pi}\sum_{n=1}^{n=\infty}[\mathrm{Sin}(n\pi/A)/n]\cos\,\left(n\left(\omega t - \frac{2k\pi}{A}\right)\right) \qquad (9)$$

2.2 Mathematical Model and Flow Chart of Maximum Power Point Tracking

The incremental conductance mathematical model is derived from the power formula which is the product of voltage and current after taking the derivative of with respect change in voltage as shown in equation (10):

$$P = I \times V \tag{10}$$

$$\frac{dP}{dV} = I\frac{dV}{dv} + V\frac{dI}{dv} \tag{11}$$

Incremental conductance MPPT method the $\frac{\mathrm{d}P}{\mathrm{d}V} = 0$ to achieve the maximum power point:

$$I + V\frac{dI}{dv} = 0 \tag{12}$$

The following conditions is used to maintain the MPPT :

$\frac{dP}{dV} = 0$ MPPT condition achieved

$\frac{dP}{dV} > 0$ Increase duty cycle to achieve MPPT

$\frac{dP}{dV} < 0$ Decrease duty cycle to achieve MPPT

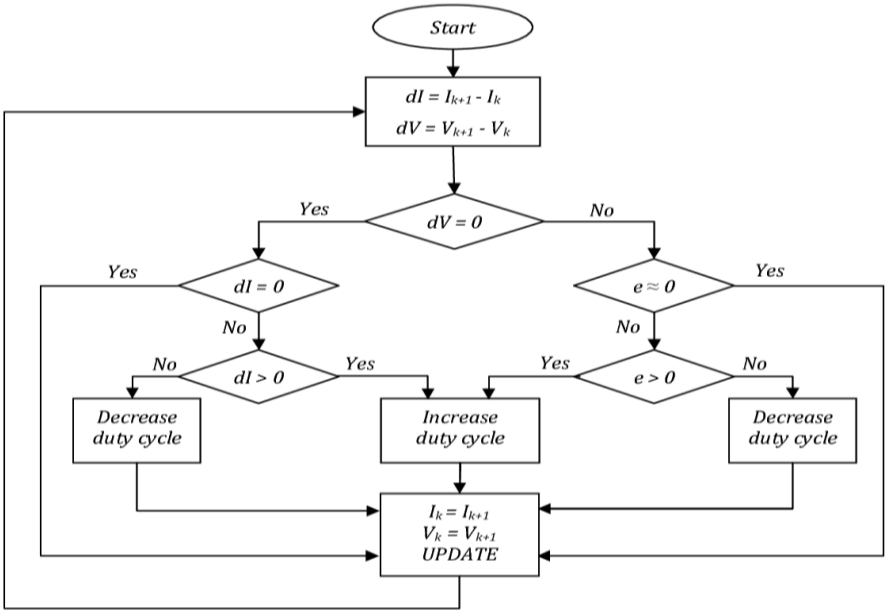

Figure 5. Flow chart to achieve MPPT

3. Simulation Model

To test and analyze the proposed system, the proposed model was simulated on MATLAB Simulink platform. MATLAB platform contains predefined blocks and functions that allow the user to implement and compile any electrical system. Moreover, it also has the ability to generate and create new blocks with user defined parameters when required. The entire setup was simulated and analyzed using MATLAB tools. The results obtained from the simulation are briefly discussed in this section.

In order to analyze the results of proposed system, four simulations were developed. Initially, a couple of solar PV panels were coupled with a single level inverter. In the second simulation, the level on inverter was increased and a single seven-level inverter was coupled with PVs. The level of inverter was increased by using cascaded inverters which are well known for mitigating harmonics at the output. In the third simulation, a couple of PVs with each having its own single-level inverter and the fourth simulation includes all these features together by coupling seven-level cascaded inverter with each of the solar panel. The primary objective, i.e., the efficiency enhancement of micro-inverters through voltage regulation and ripple compensation, was analyzed by comparing the voltage level for each of the setup. Aside from this, the partial shading effect of the systems were also analyzed in each of the mentioned simulation.

The blocks used in all of the four simulations discussed include the same internal elements with common specifications. All of the main blocks used in the simulation are discussed below.

MATLAB library contains predefined solar PV blocks; the block then has internal parameters which can be adjusted as per the user requirements. The block contains two parameters namely irradiance and temperature. The output voltage of solar PV block is DC voltage which depends upon the input value. Figure 6 shows the solar PV block used in the simulation.

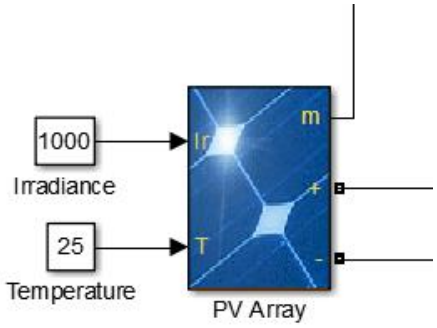

Figure 6. PV Array block, MATLAB Simulink

As shown in Figure 6, the inputs seen on the left-hand side of the image are irradiance and temperature whereas on the right-hand side, the DC output along with a measurement port to display basic parameters such as output current and voltage is displayed. As mentioned earlier, the internal parameters of the solar PV block can be adjusted as per the user requirements. Table 2 shows the internal parameters of the block.

Table 2. Simulation parameters

Parameters	Values

Start Time	0.06 sec
No. of cycles	2 cycles
Fundamental frequency	60Hz
Maximum Frequency for THD	Nyquist Frequency
Maximum Power	200.0364 Watts
Parallel strings	2
Series connected modules	1

The solar PV block has some predefined models available. The selected predefined model as shown in Figure 6 is "Chint Solar (Zhejiang) CHSM5612M (BL)-200". As seen in the Figure 7, each solar PV block has 2 parallel strings and 1 series-connected module per string. The maximum output voltage of the module is around 200.0364 Watts with Open circuit voltage rated at 37.46 V and short circuit current rated at 5.31 Amperes. The I-V characteristics of the module can also be seen for different values of irradiance and temperature by providing the irradiance value on the right side of the figure. Figure 7 shows the I-V characteristics of the module at 1000 W/m^2 irradiance.

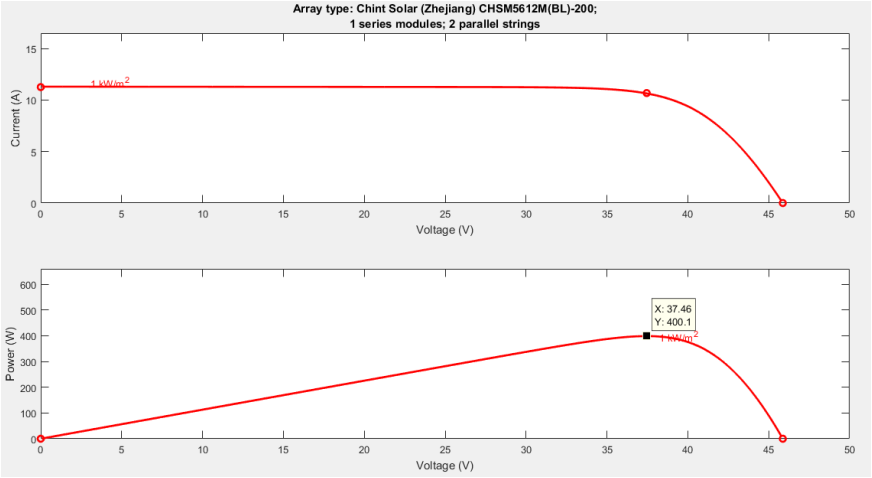

Figure 7. I-V characteristics of solar PV at 1000 W/m^2

In Figure 7, the second graph shows that the PV block is capable of providing 400.1 Watts of power at 37.46 Volts. This peak power is shifted with change in irradiance and temperature accordingly. To get the maximum power out of the solar PV block, the system needs to constantly adjust the voltage for different values of irradiance and temperature to get the maximum power output.

For this reason, an incremental conductance based MPPT converter is used to track the maximum power point. There are other techniques to get maximum output power however, incremental conductance is the most efficient and accurate technique used so far. To implement MPPT, an MPPT block has been created within the simulation which takes the voltage and current values of solar PV and runs the algorithm using several blocks. The block then generates the required pulses for the buck-boost converter to adjust the output voltage in order to keep the power at maximum point. Figure 8 shows the MPPT block along with the buck-boost converter circuit. In Figure 8, the

irradiance and temperature are the two inputs provided to the solar PV block. The output voltage is then generated as per the IV graphs shown previously.

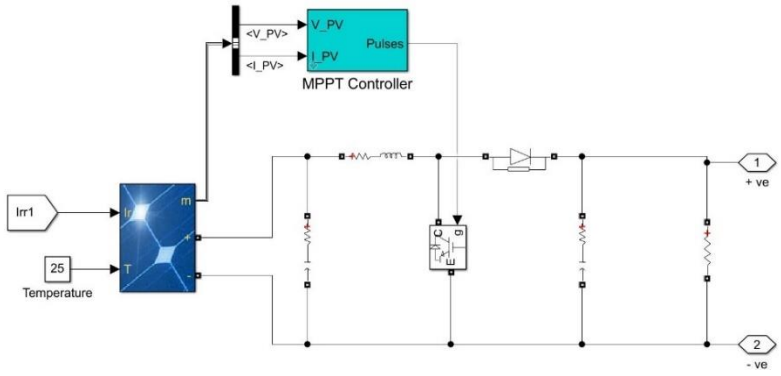

Figure 8. Solar PV module with MPPT

The buck-boost converter circuit contains some inductor and capacitors to store energy and release it by providing pulses to an IGBT. The IGBT outputs the desired voltage as per the pulses by releasing the stored energy as per the pulses received. Thus, the main control is pulses generated by the MPPT controller. Figure 9 shows the components present inside the MPPT block. V_PV and I_PV represent the solar PV's output voltage and current respectively. It represents the initially duty cycle value when MPPT is initialized. The D and P in the PWM generation box show the duty cycle and pulses respectively. This shows that the input to the PWM is the duty cycle value generated as per the algorithm which is then translated into pulses and fed to the inverter switches for generating AC.

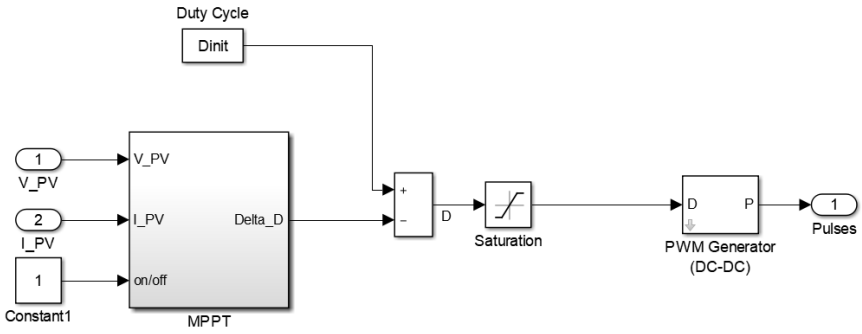

Figure 9. Internal components of solar PV block

As shown in Figure 9, the primary inputs along with an on/off switch are given to the main block which runs the incremental conductance algorithm. Aside from the voltage and current, the constant value provided by the constant block turns the MPPT ON/OFF. As seen in the figure, value '1' is given to the block to keep MPPT on. MPPT block provides Duty Cycle, denoted by 'Delta_D' in Figure 9, as its output. The output of the MPPT block is cascaded with another constant block which contains the initial duty cycle value. Thus, initially the duty cycle is a constant which changes accordingly when MPPT block starts tracking. The output duty cycle value is passed through a saturation block to control the upper and lower limits and then provided to a predefined PWM generator block as shown in Figure 9. This block generates the consequent pulses as per the given value of duty cycle and is fed to the transistor (IGBT) to control the output voltage.

The incremental conductance technique implementation is shown in Figure 10. The maximum power point is obtained when rate of change of power with respect to the voltage is zero which means that the power no longer changes with change in voltage. Therefore, the slope of the line at maximum power point would also be zero. Thus:

$$\frac{dP}{dV} = 0, where\ p = V \times I \tag{13}$$

$$\frac{d(V \times I)}{dV} = 1 + \left(V \times \frac{dI}{dV}\right) = 0 \tag{14}$$

$$\frac{dI}{dV} = -\frac{I}{V} \tag{15}$$

where dI and dV are the fundamental components of current and voltage ripples measured with a sliding time window which is lesser than the sampling time and is set at 125 milliseconds. On the other hand, I and V are the mean values of current and voltage measured by the same sliding window. The integral regulator minimizes the $\frac{dI}{dV} + \frac{I}{V}$ error and thus outputs the duty cycle correction.

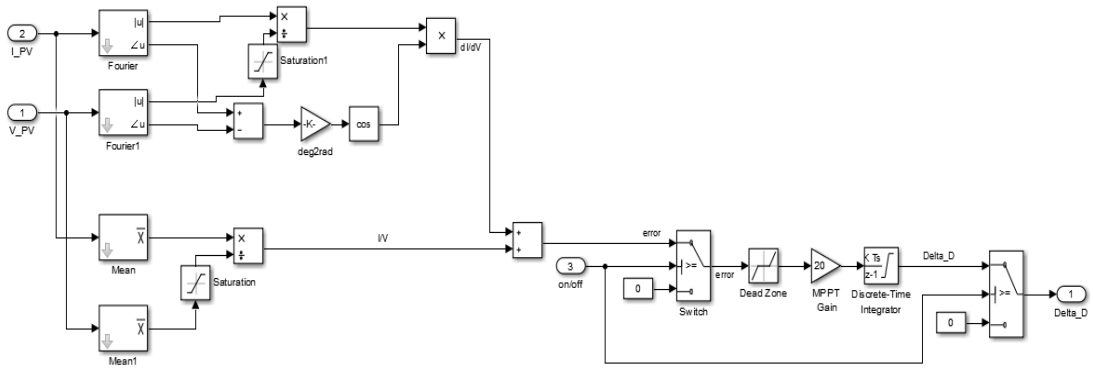

Figure 10. Incremental Conductance Algorithm Implementation

The tracking of maximum power point by the MPPT controller for the 1000w/m2 irradiance as per the I-V characteristics is shown in Figure 11.

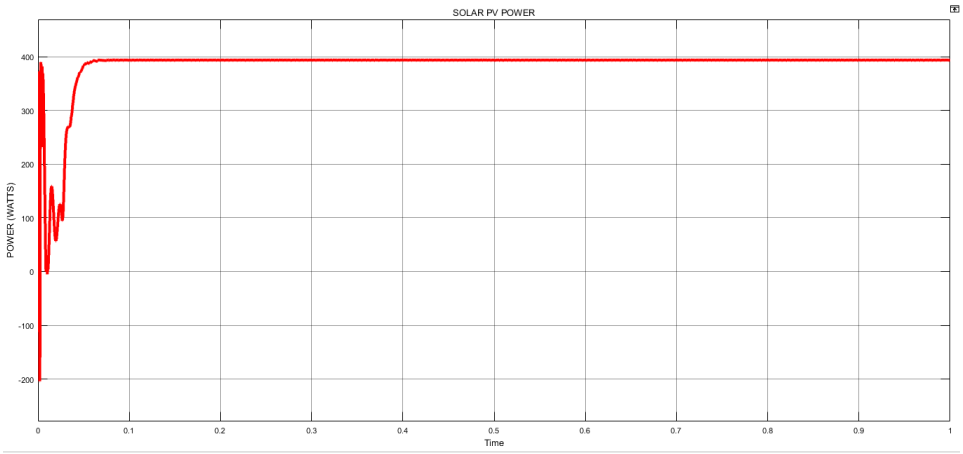

Figure 11. MPPT Tracking

The output of the solar PV is a DC in nature and has to be converted to AC in order to be integrated with the grid. The technique used for DC to AC conversion in the simulation is the H-Bridge technique. The H-Bridge used in the simulation is shown in Figure 12. As shown in the figure, the four IGBT diodes are connected in order to form an H-bridge and the outputs taken out enables the system to generate an alternating sequence.

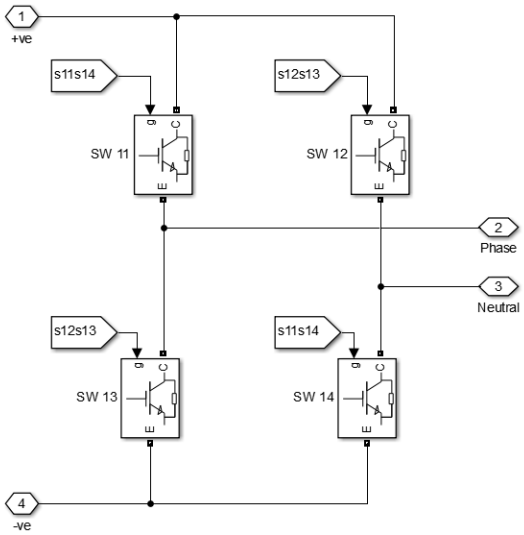

Figure 12. Inverter internal components (H-bridge formation)

There are four IGBTs which each of them getting pulse signal from the inverter controller. The IGBTs connected diagonally and have the same input as shown in the figure, i.e., SW11 and SW14 have the same input pulses whereas SW12 and SW13 have the same input. The transistors connected below one another such as SW11 and SW13 should not be turned on at the same time to avoid short circuiting. Moreover, the switching ON/OFF of upper two IGBTs only and switching off of lower two IGBTs and vice versa would result in zero voltage output. For this reason, the sequence of switching shall be carried out in such a way that only diagonally connected transistors are turned on and they are given enough time to switch off before the other two transistors are turned on. The datasheet of the transistors being used must be consulted before implementing the system and switching frequency must be set accordingly. For the controller circuit of the inverter, the Sinusoidal pulse width modulation (SPWM) technique is used. As shown in Figure 13, a reference signal block with unity amplitude and 50 Hz frequency is provided to the control block. The control block then uses two saw tooth wave generators and compares it with the input reference signal. The gain block is used to equally divide the input signal for positive and negative half cycle. The consequent pulses are then provided to diagonally connected IGBTs as shown in Figure 8 to convert the DC signal to AC. The frequency of the pulses is set to 2.5kHz.

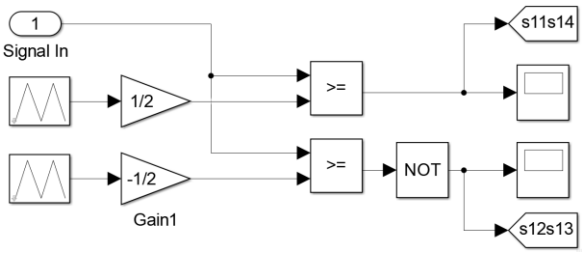

Figure 13. Inverter control unit

As discussed earlier, in order to analyze the proposed system under different conditions, two simulations were made with each one having different solar PV and micro-inverter configuration. The blocks described in Figure 13 remains the same in all of the simulations. The output of seven solar PV systems is connected to a single-level inverter. The internal components of each of the solar PV system are the same as discussed. Each of the solar PV has the ability to generate roughly 400 Watts at maximum power point. Each of the solar PV is also connected with a MPPT which is responsible for each individual PV to navigate to its maximum power point with changing irradiance. Another reason for adding MPPT with each of the solar PV module is to make sure that the parameters affecting the system performance do not pertain to the solar PV.

4.1 Case I: Central Single Level Inverter

The central single-level inverter has an RL load attached to its output. The current and voltage waveforms of the load are being analyzed to see how the setup influences the output values. In Figure 14, the irradiance values of each solar PV panel are also shown. The developed simulation allows the user to set a unique value for each of the PV module. The simulation was first tested with all solar PVs at maximum irradiance. Later, some of the PV modules were shaded by changing their respective irradiance values to zero.

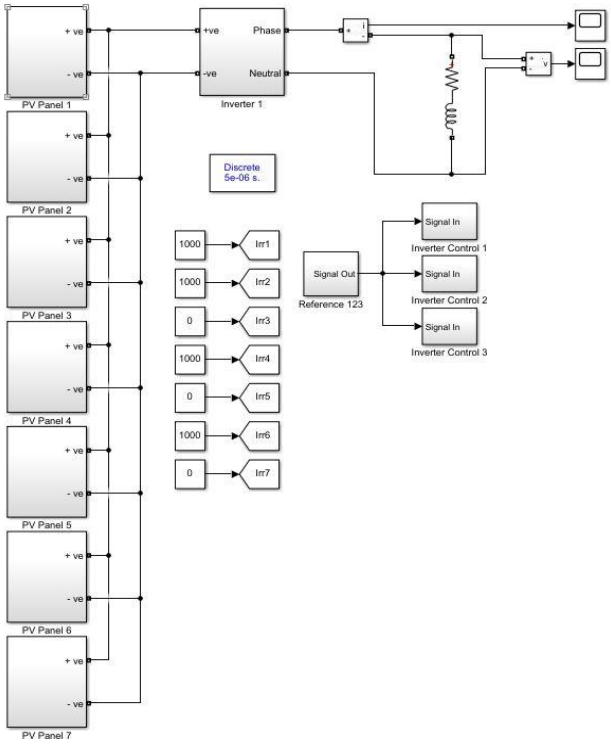

Figure 14. Central single level inverter

4.2 Results and Discussions

Figure 15 shows the load current of the setup illustrated in Figure 14. In this setup, all seven solar PV systems were operated at maximum irradiance values and thus producing maximum power. The current waveform obtained shows ripples. Moreover, the current delivered to the load at this point is approximately 0.25 mA.

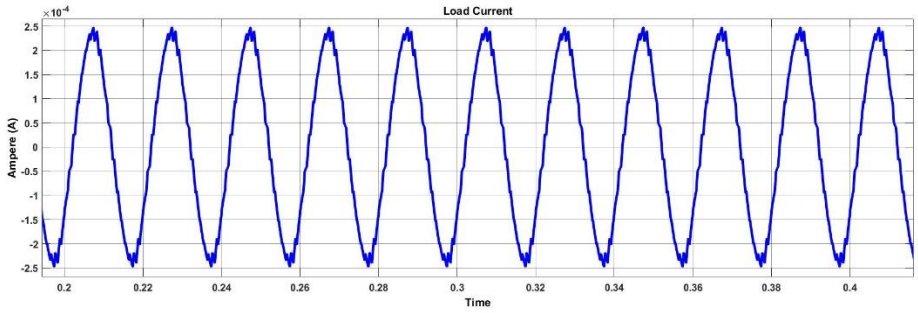

Figure 15. Single-level central inverter load current with full irradiance

The harmonics in the current waveform were analyzed by using the FFT tool available in Simulink. Two cycles of the obtained waveforms were checked with fundamental frequency at 50 Hz and maximum frequency at 1 kHz. The total harmonic distortion measured at these parameters showed THD % at 4.65. The voltage waveform of the load was also analyzed for presence of harmonics for reference purposes. The voltage waveform of the load for a single level central inverter is shown in Figure 16. Due to presence of inductive component, the sinusoidal pattern can also be observed in the voltage waveform as well. The peak-voltage measured with this setup as seen in Figure 16 is about 84 Volts.

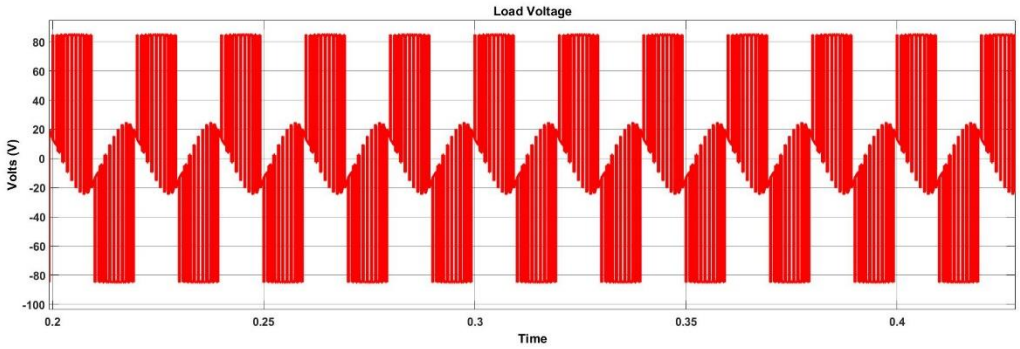

Figure 16. Voltage waveform for single-level central inverter at full irradiance

The presence of inductive element in the load compensates the harmonic presence up to some extent which can be seen in the Figure 16. However, the waveform would still have high THD percentage. Aside from that, the single level inverter is the primary reason of high harmonic distortion as it produces square output. The pulsating signal somewhat makes it equivalent to a sinusoidal wave which is why the current harmonics are reduced significantly.

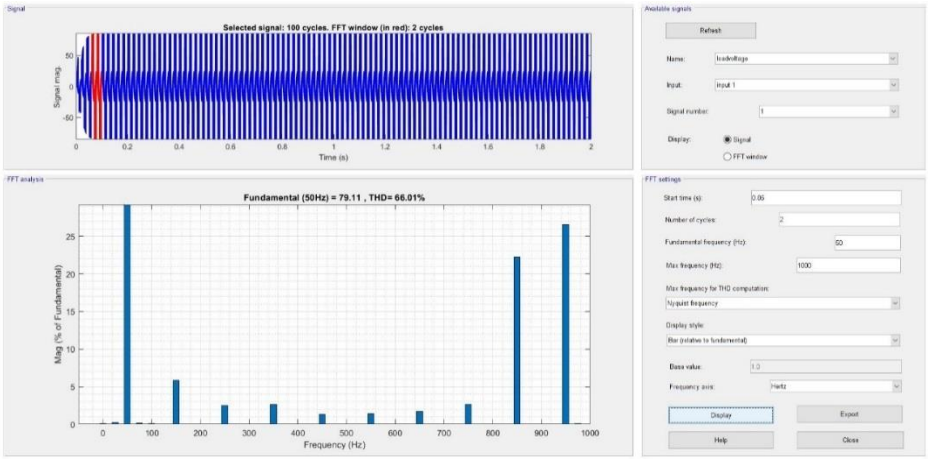

Figure 17. THD load voltage for single-level central inverter at full irradiance

With the same parameters as set for current waveform, the FFT analysis of the voltage waveform gives 66.01% THD level. The reason for this high value of THD is explained above. It is worth mentioning that the waveform for all the four simulations for THD analysis was taken for 2 cycles starting from 0.06 seconds. This delay in observing the waveform lets the waveform to stabilize as the inductor and other active components stabilize and depict a steady state response of the system.

The next simulation was again tested under the same parameters and conditions. This time, out of seven PV panels connected in parallel for high power delivery, three panels have zero irradiance. In the real time, this would depict partial shading of the solar PV. With the central inverter, the overall performance of the PV system is compromised under such conditions. Figure 18 shows the load current waveform for partially shaded solar PV system.

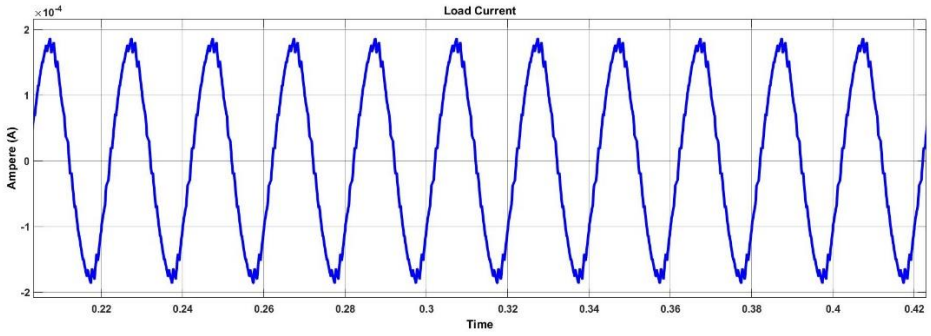

Figure 18. Single-level central inverter load current with partial shaded setup

The current waveform is mostly similar to that shown previously with full irradiance of all solar PVs. However, it can be seen in Figure 18 that the amplitude of the current has been reduced. Due to partial shading, the amplitude of both current and voltage waveforms has been reduced to a significant level. Previously, with full irradiance, the current amplitude was measured at 0.25mA whereas with three of the solar PVs with zero irradiance, the current level falls down to about 0.18mA.

The same effect can be noticed in the voltage waveform as well. For the previous value measured at 84 volts peak, the current value due to partial shading has decreased to about 63 volts. It can be seen that neither the current nor the voltage waveform has changed much but the amplitude of both the waveforms have been mitigated approximately up to 25%.

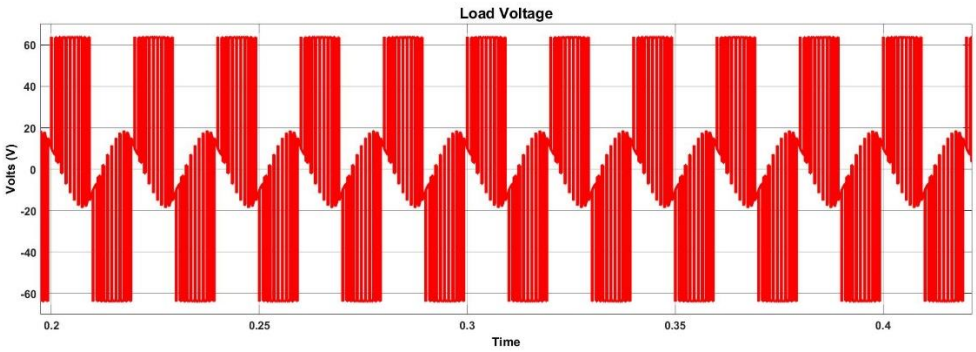

Figure 19. Voltage Waveform for single-level central inverter with partial shaded setup

Virtually, the waveforms generated under both, partial shaded and full irradiance conditions only show decrease in amplitude but no additional ripple distortion. To test the same theory, FFT analysis of both the waveforms were measured again.

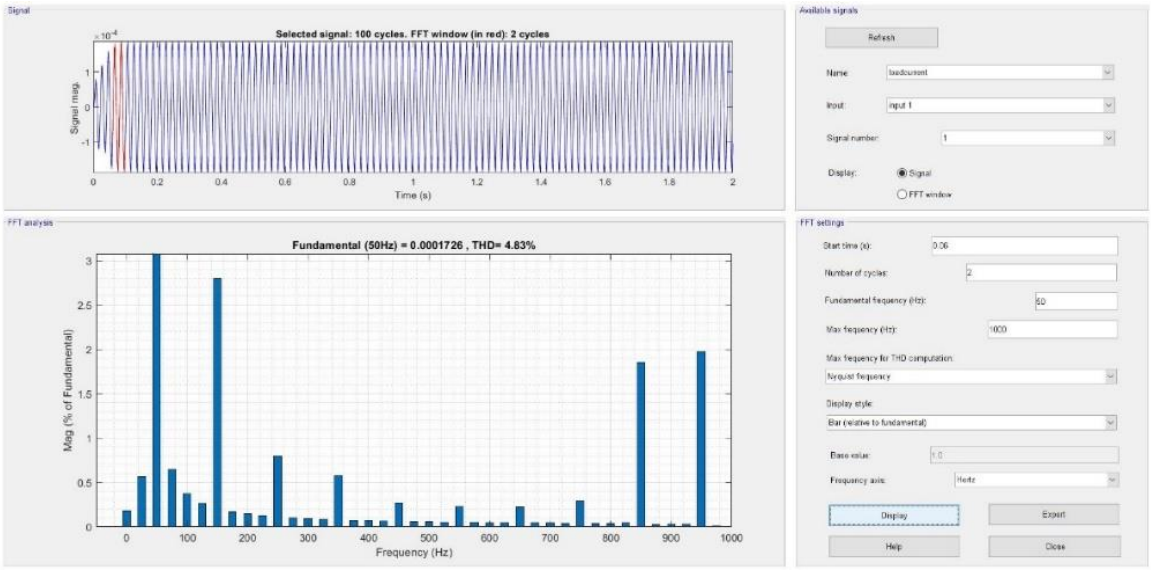

Figure 20. THD of load current for single-level central inverter with partial shaded setup

FFT analysis of current waveform shows that partial shading of solar PV panels with central inverter also enhances harmonic distortion. Even though the increase is not that significant in the simulation, in real time, under different losses and manufacturing defects, these harmonics can increase even more. Compared to the previously measured 4.65% THD, the partial shaded setup shows 4.83% THD for the current waveform.

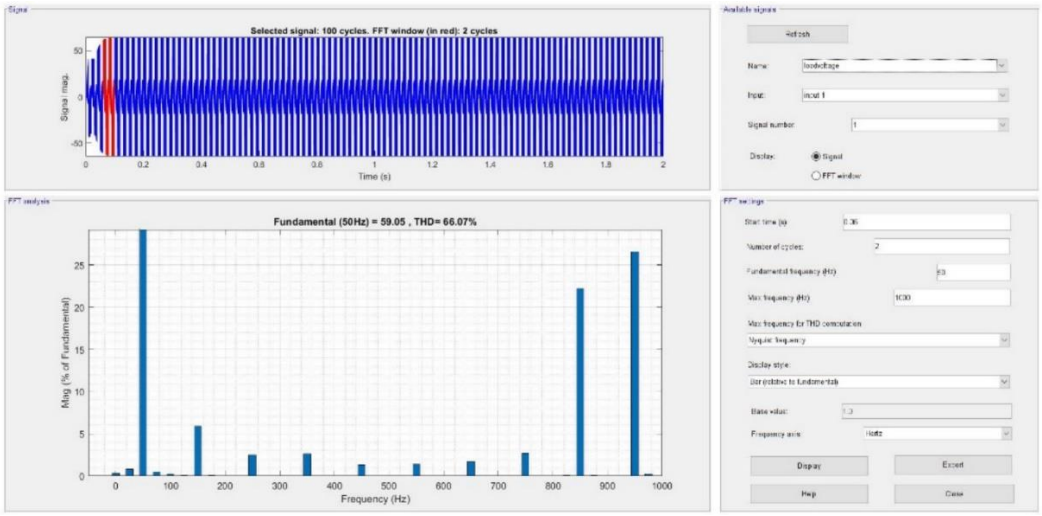

Figure 21. THD load voltage for single-level central inverter at partial shaded setup

The voltage waveform on the other hand also shows the impact of partial shading. As shown in Figure 21, the voltage harmonics previously measured at 66.01% at full irradiance increased to 66.07% under partial shaded conditions. This happens due to the reason that some of the solar PVs not being generating any power produced dip in the delivered power. The extra power required is thus provided by the other solar PVs which in turn affects the output of the inverter and slightly increases harmonic distortion. In this scenario, the considered primary parameter is the voltage level rather than the harmonic distortion. Even though the increase in harmonics is negligible, but the decrease in voltage peak can have prominent impact on all the elements of the system especially load.

4.3 Case II: Cascaded Multi-Level Micro Inverter

The last step in the entire proposed work is to add the two performance enhancement techniques and to look for the results and normal and partial shaded conditions. For this purpose, the cascaded inverters were coupled with each individual PV modules under the same parameters and conditions. The simulation for this purpose as developed in Simulink is shown in Figure 22.

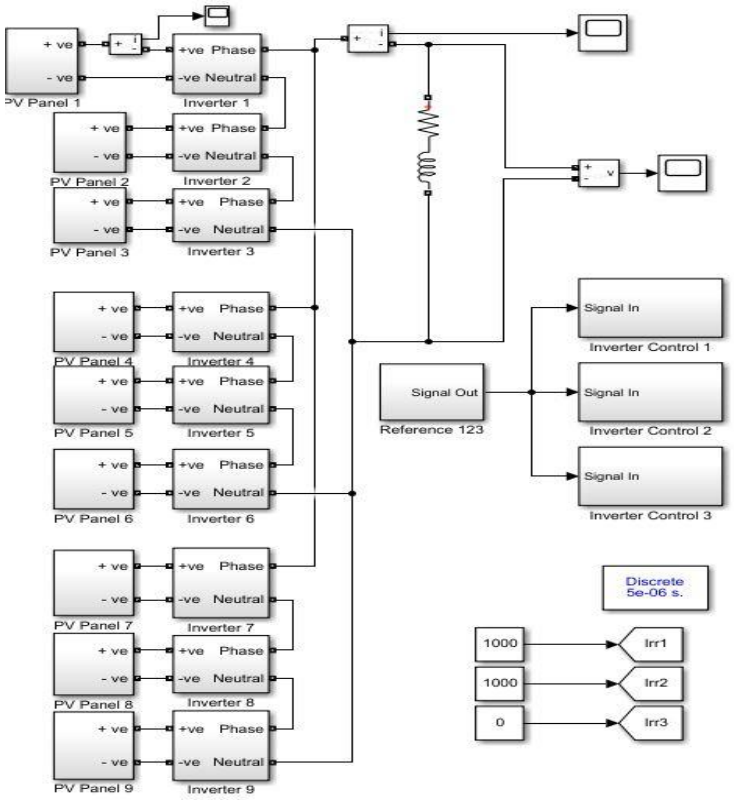

Figure 22. Cascaded micro inverter

5. RESULTS AND DISCUSSIONS

First of all, the main performance parameter which is the current waveform was analyzed. As shown in Figure 23, the current waveform shows high resemblance to an actual sinusoidal waveform. Under full irradiance conditions, the current amplitude was measured at about 7 mA.

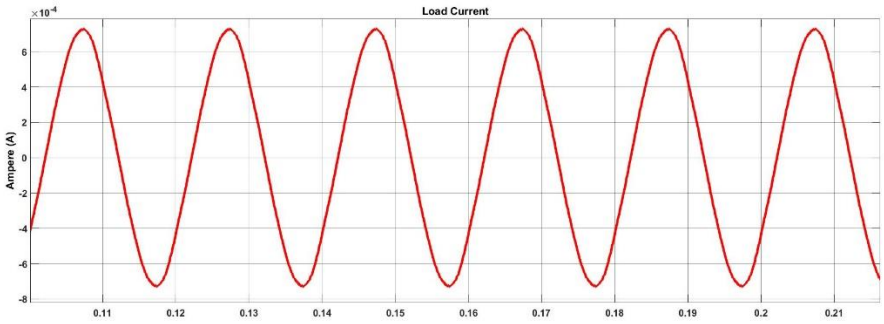

Figure 23. Current waveform of cascaded micro-inverter at full irradiance

The corresponding THD of the current waveform under consideration is shown in Figure 24 with cascaded multi-level inverter, the THD is significantly reduced to about 2.66% which reveals that this setup with cascaded micro-inverters proves out to be the best at ripple compensation through reducing harmonics in the system.

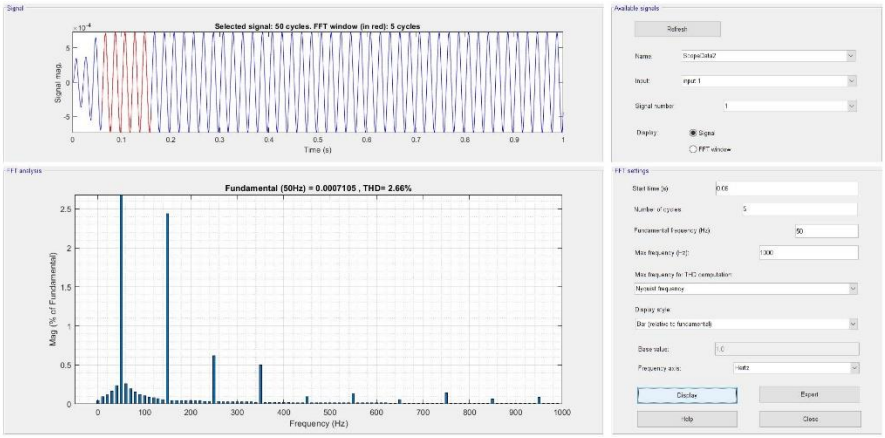

Figure 24. THD of load current for cascaded micro-inverter at full irradiance

The voltage waveform on the other hand also shows better results both in terms of voltage regulation and ripple compensation. The voltage level is maintained at 250 volts with the waveforms appearing to be smoother than any of the previously simulated systems. The THD analysis also supports the argument. Compared to the 66.01 % of the single level centralized inverter, this setup brings down the THD in voltage waveform to a staggering 23.35%.

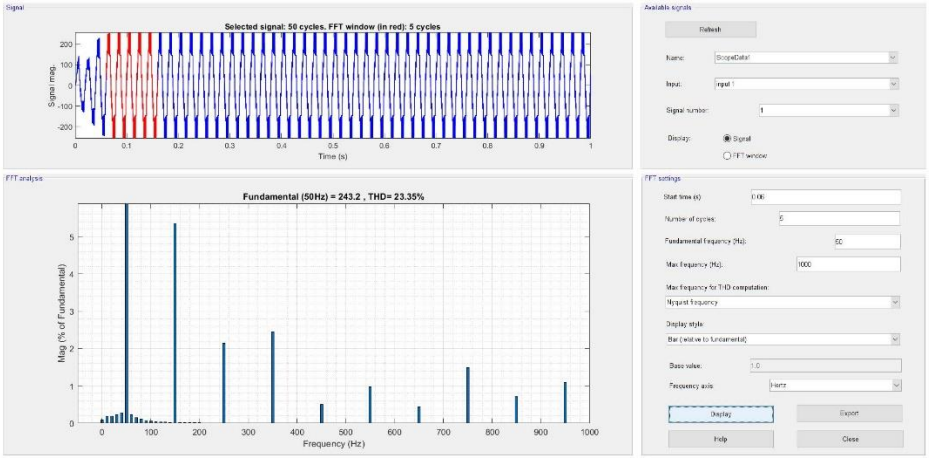

Figure 25. THD of load voltage for cascaded micro-inverter at full irradiance

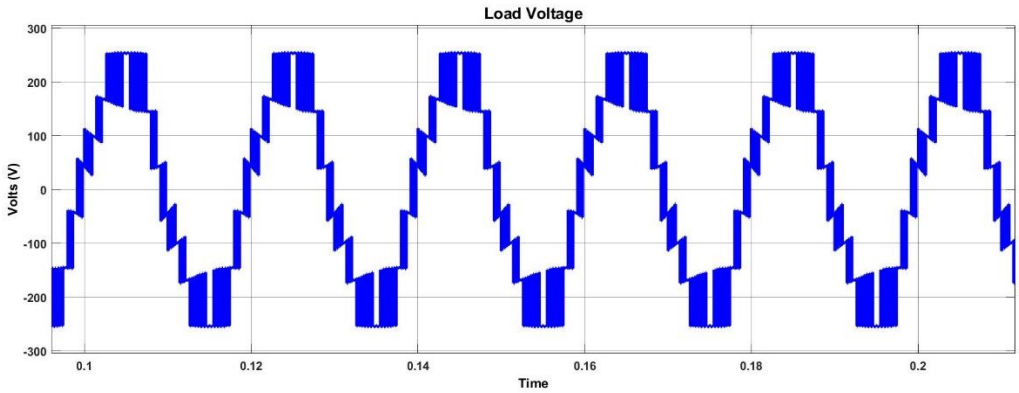

Figure 26. Voltage waveform of cascaded Micro-inverter at full irradiance

To test the system under partial shaded conditions, one of the three PV modules is provided with zero irradiance. However, due to the inclusion of cascaded multilevel inverter for each of the micro-inverter coupled with the solar PV modules, the amplitude of both current and voltage remain at the same level which depicts that partial shading effects can be mitigated significantly through the proposed technique.

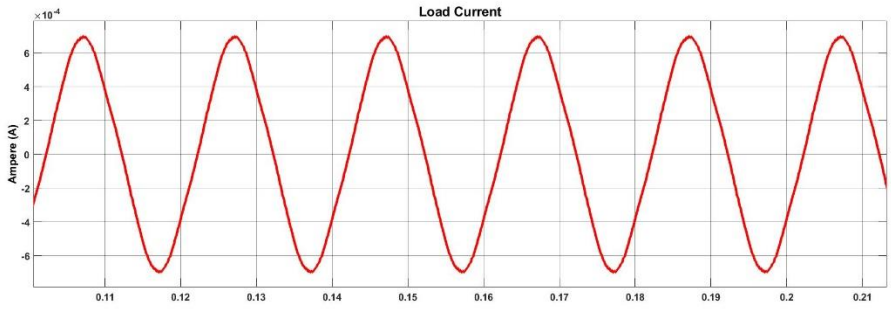

Figure 27. Current waveform of cascaded micro-inverter with partial shaded setup

The current waveform is shown in Figure 27 is measured under partial shaded conditions of cascaded multilevel micro-inverter topology. Even though the irradiance of one of the three modules is completely zero, the current amplitude maintains its value at 7 mA.

The voltage waveform is of vital importance in terms of partial shaded conditions. As seen in the previous results, the voltage level is the most affected variable for such conditions. However, this affect is also been taken care of with the proposed method. As shown in Figure 28, the partial shading does not impact the voltage level of the system output and maintains it at 250 volts.

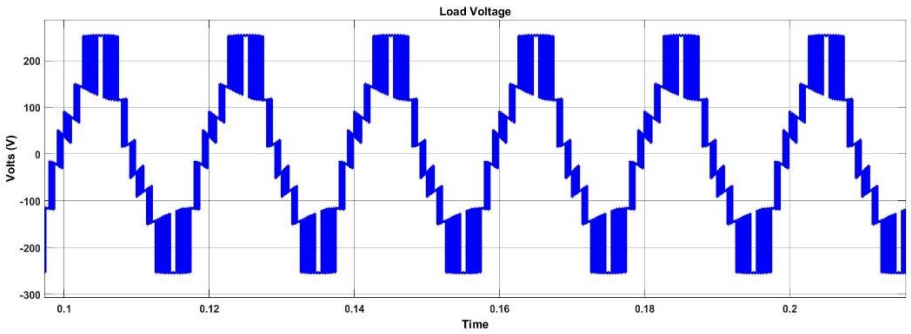

Figure 28. Voltage waveform of cascaded micro-inverter with partial shaded setup

However, the THD of the current and voltage waveform under partial shaded conditions do get affected. Under these conditions, the current THD increases to 4.82% whereas the voltage THD reaches 29.8%. Figure 29 and 30 show the voltage and current THD analysis respectively.

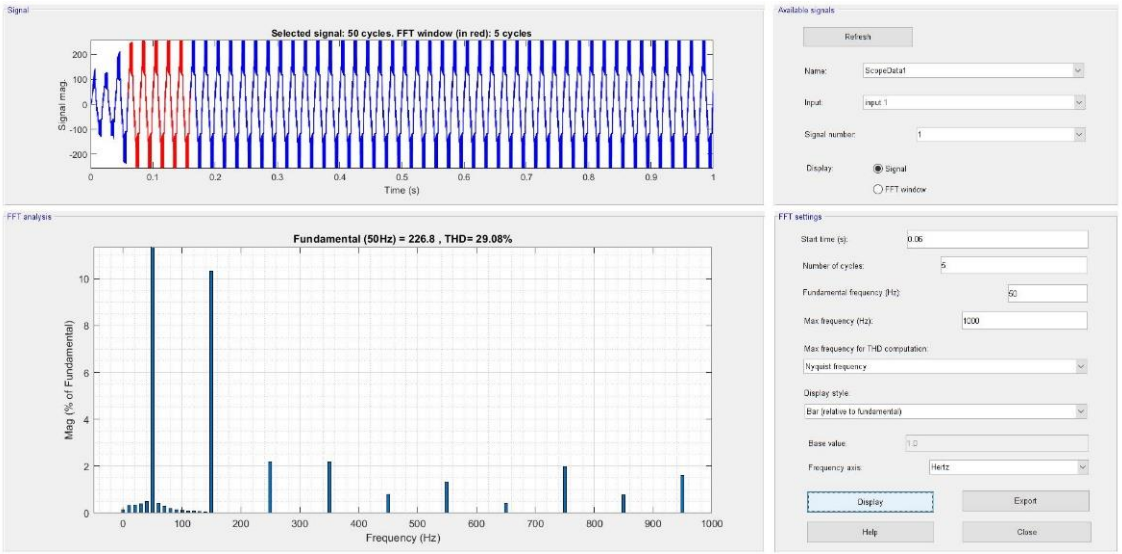

Figure 29. THD of load voltage for cascaded micro-inverter with partial shaded setup

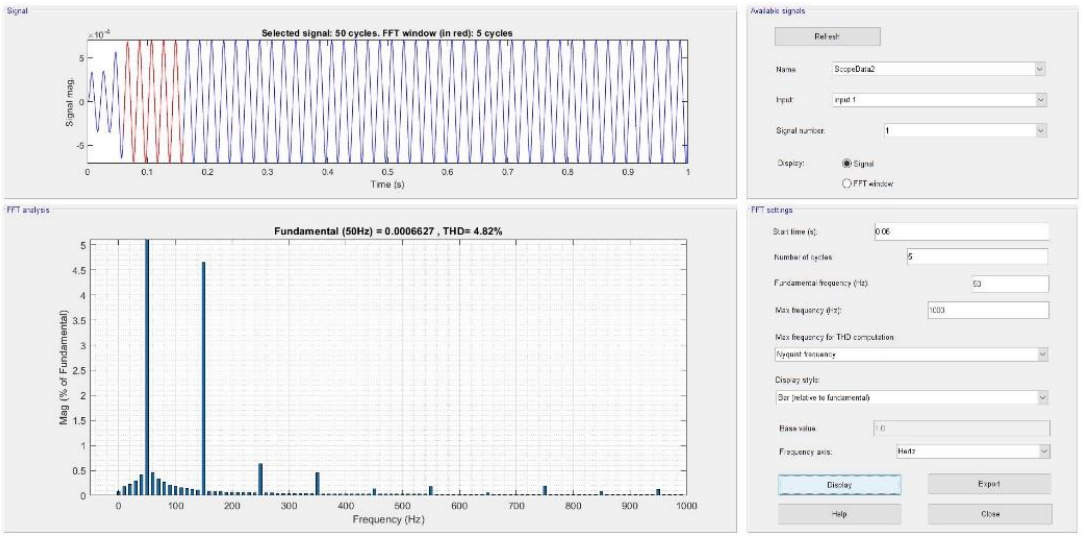

Figure 30. THD of load current for cascaded micro-inverter with partial shaded setup

The results obtained reveal that through coupling each of the solar panel with its own micro-inverter and by adding the cascaded inverter topology, the overall performance of the system can be enhanced significantly. Comparison can be made in a single level central inverter and a multi-level cascaded micro-inverter. The voltage harmonics, current harmonics, and voltage and current amplitude mitigation can be controlled significantly by using the proposed method. The harmonic mitigation in this aspect accounts for the ripple compensation that occurs during the DC to AC conversion whereas the partial shading effects can become negligible with the proposed method.

It is also revealed from the results that the partial shading does increases harmonics with cascaded inverters. However, the impact is still very limited compared to a single level inverter. Even though the overall THD of both current and voltages increase under partial shading however, the THD

percentage remains within the IEEE defined limits. Table 3 shows a comparison between these two cases.

Table 3. Comparison at full and partial irradiance

	Case I	Case II
Voltage Amplitude at full irradiance (Volts)	84.00	250.00
Voltage Amplitude at partial shaded (Volts)	63.00	250.00
Current Amplitude at full Irradiance (mA)	0.25	7.00
Current Amplitude at partial shaded (mA)	0.18	7.00
Current THD at full irradiance (%)	4.65	2.66
Current THD at partial shaded (%)	4.83	4.82
Voltage THD at full Irradiance (%)	66.01	23.35
Voltage THD at partial shaded (%)	66.07	29.08

6. CONCLUSION

This paper proposes the methods of reducing total harmonic distortion and voltage ripples in single level and multi-level micro inverter for the efficiency and reliability enhancement of photovoltaic panels and micro inverters. Two different cases are carried out to calculate the total harmonic distortion and voltage ripples. The integration of micro inverter with PV panel at partial and full shading conditions has been studied. From the results, it is clear that the total harmonic distortion is reduced to 44.01 % in case of cascaded multi-level micro inverter and voltage and current amplitude is compensated in the system and is energy efficient and it shows that by changing switching angles, combination of strings, fundamental frequency and number of cycles, the cascaded multilevel system enhances and improves its reliability.

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