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Reliability Analysis and Power Dissipation of Quantum Dot Cellular Automata Circuits for Next Generation Computing

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ABSTRACT

Quantum Dot Cellular Automata (QCA), an emerging Field Coupled Nano computing which is the new paradigm of computation has to be analyzed for reliability and thermal stability and power dissipation. The main focus of the research paper is to analyze a high input majority voter based 3 to 8 decoder for reliability using Bayesian network at the circuit level. The charge configuration flow indicates the reliability of the data transmitted and hence the behavior of the QCA Circuits has been analyzed. The Casual Direct Acrylic graph is used to analysis the behavior of QCA circuits. The power dissipation of the QCA circuits is also analyzed using QCADesigner-E tool and Bayesian networks are generated using dagitty tool.

Keywords: Quantum Dot Cellular Automata, QCADesigner, dagitty, QCADesignerE.

I. INTRODUCTION

As the Field Coupled Nano Computing technologies like Quantum Dot Cellular Automata has evolved [1-4], the circuits which are designed using them considerably needs to tested for reliability. Bayesian networks are used for checking the reliability of QCA Architecture by defining the conditional dependencies between the variables involved in the System. Bayesian networks are probabilistic directed acyclic graphical model that gives the Joint and conditional Probability occurrences between the variables and the Nodes.

In this Paper the main focus is on finding the Probability that the exact output signal will occur by checking the connectivity between the variables and nodes. The pre proposed work of 3 to 8 Decoder using high input majority voter in QCA technology has been utilized here to study the reliability and power dissipation. The novelty of the proposed work is that the designed QCA circuits are tested for reliability using Direct Acrylic Graphical methods

which studies the casual dependency between the different Quantum Cells of the The tools used for reliability analysis is GATIT and for power dissipation is QCADesignerE [10] [11].

II. QCA STRUCTURES

The QCA cells has quantum wells in which the electrons can be deposited which can occupy the antipodal sites and represents the binary logic '0' and '1'. The cells be connected together to carry the signal from one circuit to another using different configurations such as Wire, Inverter and Majority Voter. The Majority Voter is similar to the gate structures used in the Conventional Complementary Metal Oxide Semiconductor Field effect transistor. The primary majority voter is a three-input majority gate, researchers had figured out using high input majority voters which can simplify the circuit at the layout level [1-4]. The Figure 1 represents the QCA cells with the polarization of -1 and +1 to represent binary values of '0' and '1'. The Figure 2 represents wire which is used as line between the input and output and as interconnects in high configuration architectures.

Fig 1. QCA Cell

Fig 2. Wire

The Figure 3 represents inverter which can be used for inversion and also in coplanar wire crossing as even tap and odd tap for signal transmission. The Figure 4 represents a three-input majority voter with the input terminals and the output terminal and an intermediate cell which is stimulated by the changes of states of the inputs A, B and C. The Polarization of any one of the terminals is fixed at either -1 or +1 to represent AND and OR gate using the following equation of the majority voter.

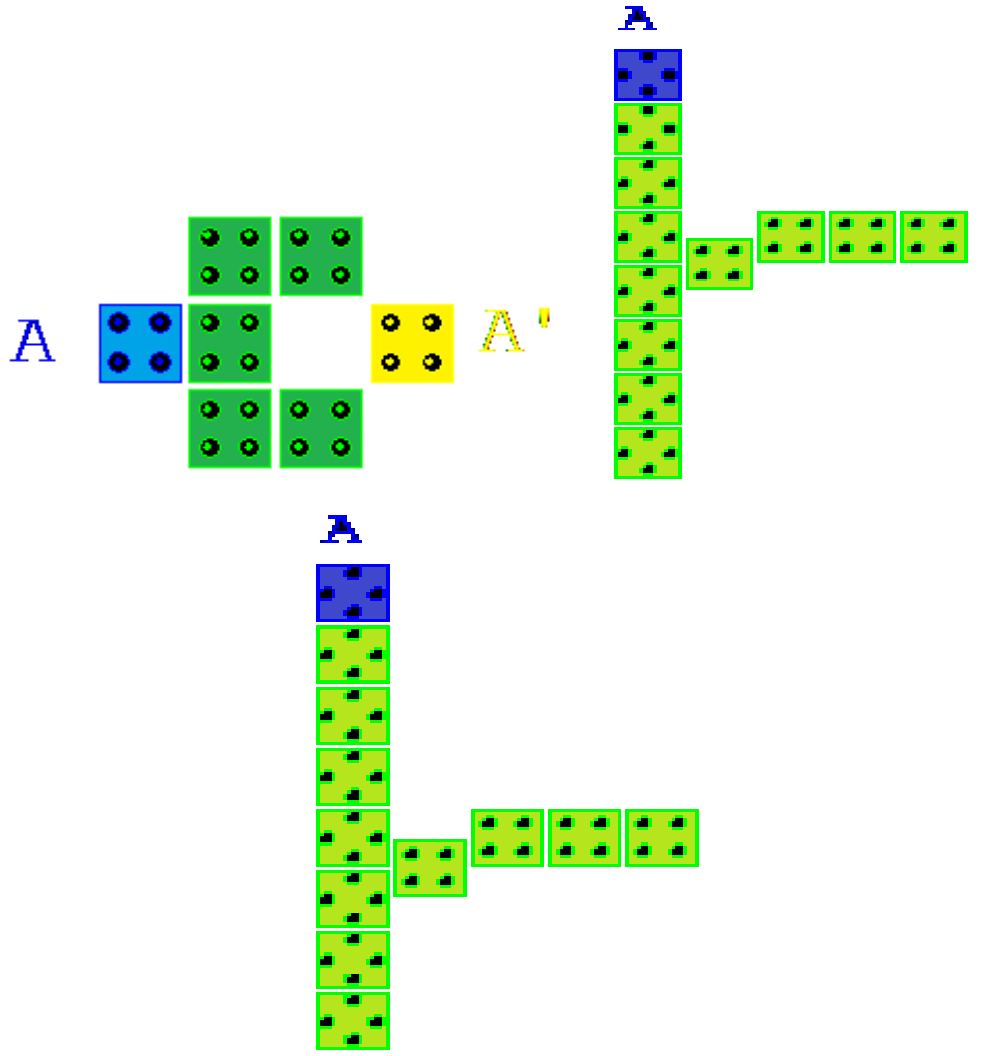

Fig 3. Inverter, Even tap and Odd Tap

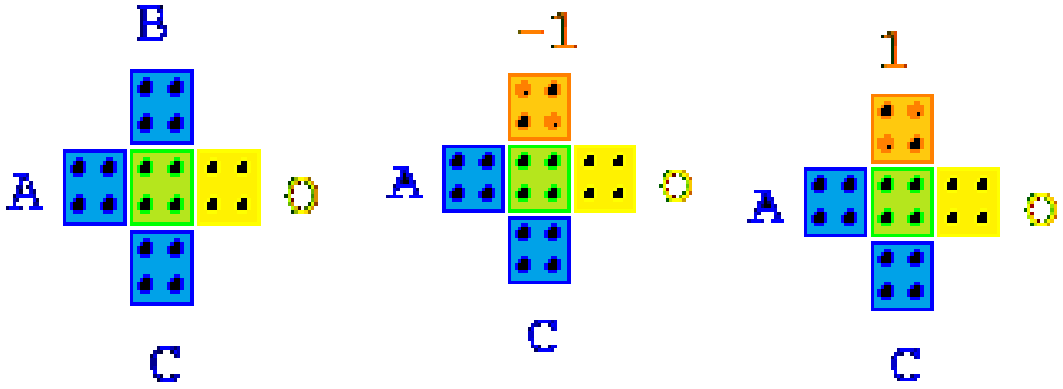

Fig 4. Three Input Majority Voter with AND gate and OR gate

For a Five input Majority Voter the input terminals are A, B, C, D and E, where the polarization has to be fixed for two inputs either as -1 and +1 to represent AND and OR gate.

The power gain and dissipation has been studied in [7], in which the power in the QCA cells is provided by the clock pulses. There are four phases of Clock which are Switch, Hold, Release and Relax. In this Paper the probability of occurrence of the correct signal is considered, whereas the probability of occurrence of clock pulses is not considered in this work.

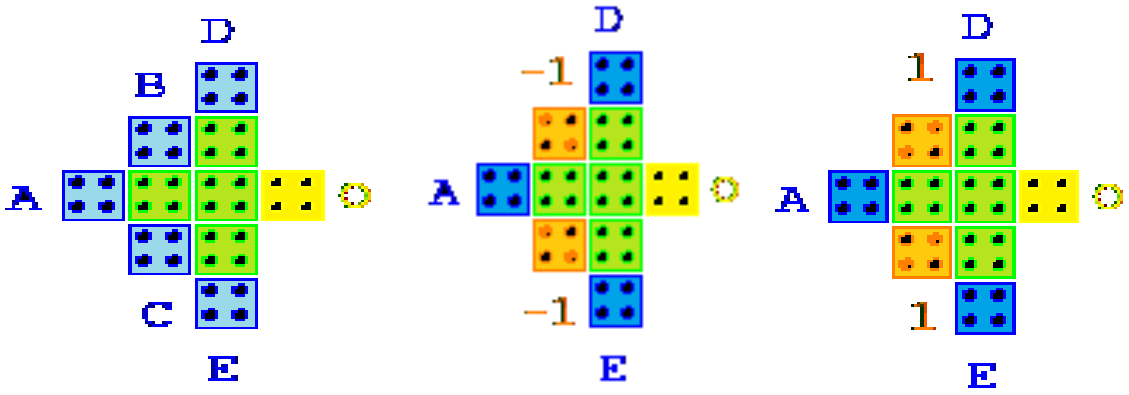

Fig 5. Five Input Majority Voter with AND gate and OR gate

III. PROBABILISTIC MODELING OF QCA CIRCUITS

The uncertainty that exists in the computing of QCA circuits can be studied by hierarchical modeling using Bayesian network. The reliability of a QCA circuit has to be studied by using the Boolean logic of the circuit and also by the probabilistic nature of the functions involved [9]. The probabilistic modeling of QCA circuits has been widely studied by Saket et al., and the authors has utilized a Full adder to study the stability using Bayesian Network. The Bayesian model and Macromodel of Three input majority gate presented in [9] has been presented in Figure 6.

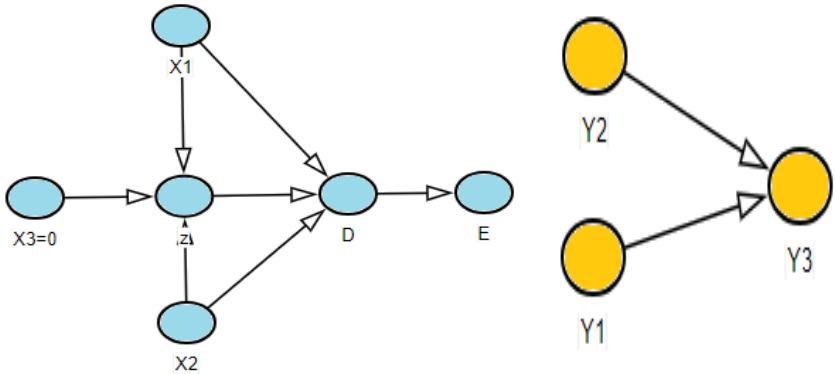

Figure 6. A three Input Majority Gate (a) Bayesian model of QCA layout (b) Bayesian network of macromodel block diagram.

The output of a Majority Voter is determined by the polarization of the output variable, which is probabilistic nature, such as P(X=0) or P(X=1). Again, the output polarization or probability of exact occurrence depends on the temperature and the ground state configuration which is maintained by the adiabatic clocking Phases of QCA [9]. The nodes represent the variables and the link between the different nodes gives the direct dependencies between the Variables. The proposed work concentrates on hierarchical modeling of QCA circuits since the vector engines such as bistable and coherence vector simulation engines focusses mostly on the state of the vectors. The QCA circuits are Unidirectional since the signal flows from Input to the Output and hence casual DAG can be used to study the modeling [10].

In Fig 7, the Bayesian model of Five Input Majority gate in QCA technology has been created using dagitty [10], which utilizes the Casual dependency between the variables and the nodes. The correlation graph in Fig 7 (c), represents the conditional Probability of the various nodes of a Five Input Majority Voter with the variables in unidirection. In a Five input Majority voter, there are Five input nodes such as A, B, C, D and E and one output node which is driven by the Majority logic Function as shown in Equation 1.

$$F= M (A, B, C, D, E) = ABC+ABD+ABE+ACD+ ACE+ADE+BCD+BCE+BDE+CDE \quad (1)$$

The Bayesian modeling of the Five input Majority gate as represented in Figure 7 can be expressed in terms of the Joint Probability distribution as in Table I.

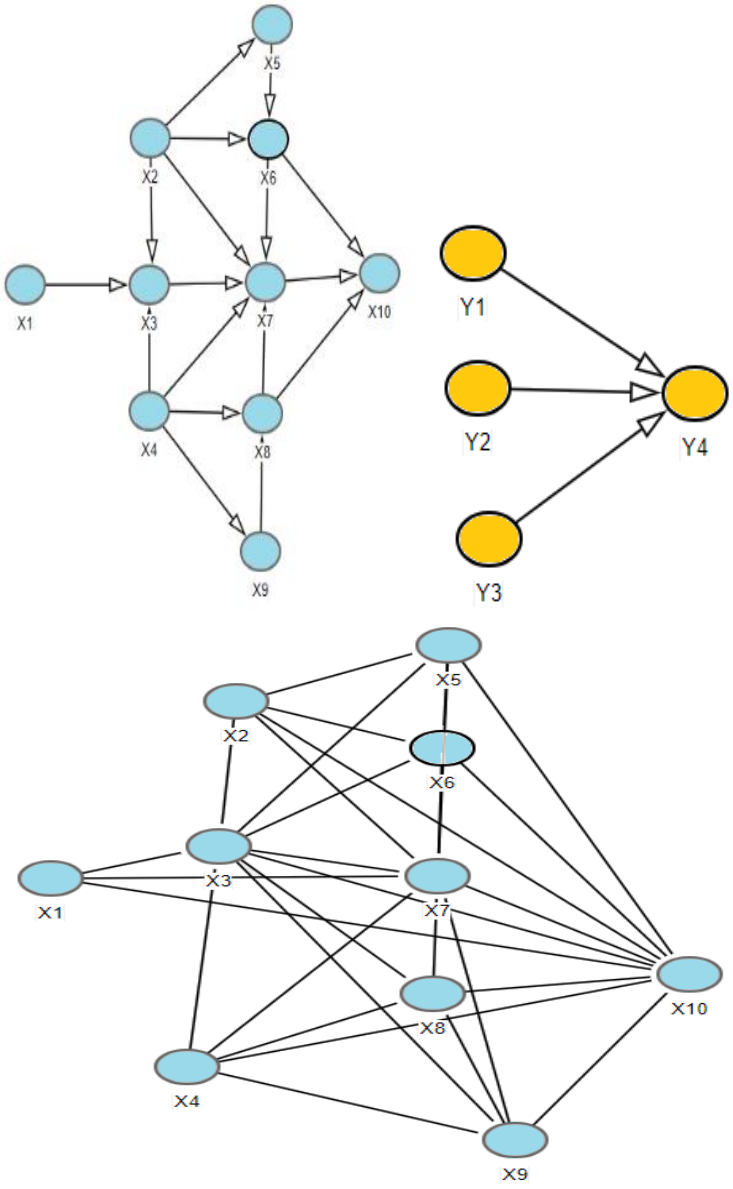

Figure 7. A Five Input Majority Gate (a) Bayesian model of QCA layout (b) Bayesian network of macromodel block diagram (c) Correlation Graph of a Five Input Majority Gate

Table I Joint Probability Distribution

Probability Dependency between the nodes	The Probability of correct/erroneous output
P (x10|x9, x8, x7, x6, x5, x4, x3, x2, x1) P (x9| x8, x7, x6, x5, x4, x3, x2, x1) P (x8| x7, x6, x5, x4, x3, x2, x1) P (x7|x6, x5, x4, x3, x2, x1) P (x6| x5, x4, x3, x2, x1) P (x5| x4, x3, x2, x1) P (x4| x3, x2, x1) P (x3| x2, x1) P (x3| x2, x1) P (x2| x1) P (x1)	P (x10, x9, x8, x7, x6, x5, x4, x3, x2, x1)

Similarly, the conditional joint probability between the Child and the Parent nodes can be given by considering the random variable X10, whose parent node is X6, X7, X8 and it is independent of the nodes X5 and X9 which is represented by the correlation graph as in Fig 7(c). The Probability of correct output also depends on the radius of the neighboring cells. The minimal factored representation for the Bayesian Network [8] is given by equation 2.,

$$P(X) = P\ (x_k\ |pa(x_k)) \qquad (2)$$

The Pre-proposed work in [6] is a 3 to 8 decoder with enable input using Five Input Majority Voter with inputs A, B and C and Outputs from OUT 0 to OUT 7 as given in Figure 8 with both schematic and QCA layout which is drawn using QCADesigner [5].

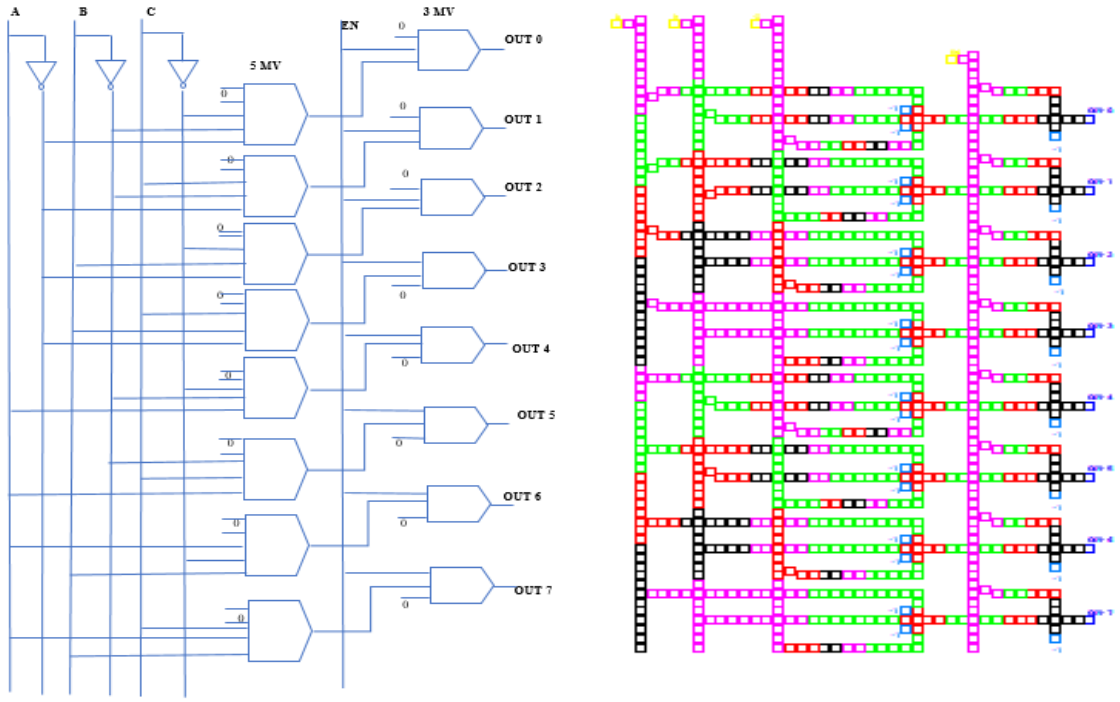

Figure 8. High Input 3 TO 8 Decoder Schematic and QCA Layout

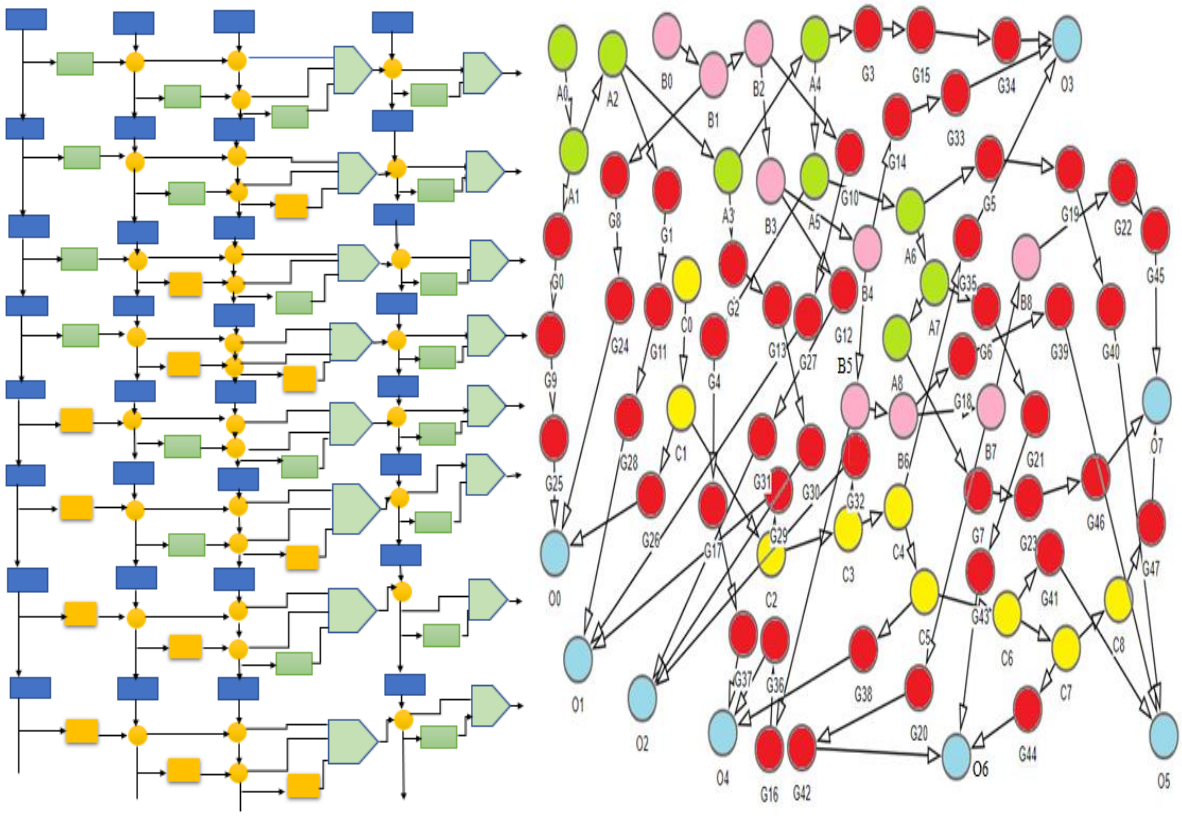

Fig 9. Circuit level QCA Layout and Macromodel Bayesian Network

Figure 9 represents the Circuit Level QCA Layout which is derived from the schematic of 3 to 8 decoder represented in Figure 8. The Macromodel is a collection of cells represented in the QCA layout level. Inorder to check the reliability of the high input 3 to 8 decoder [6], the Circuit level Layout and Macromodel using Bayesian Network has been created using [10]. The polarization of each QCA cell is computed and the probability of the layout and macromodel are more or less the same at different Temperatures [9]. The Macromodel Bayesian network has the parent nodes represented interms of A_n, B_n, C_n and the child nodes in terms of G_{pq} and output nodes as O_m, where are n, m, p, q are the arbitrary constants which defines the number of times the variables can exist. By the Macromodel modeling using Bayesian Network, the nodes which are responsible for the maximum Likelihood can be identified. The maximum likelihood node represents the probability of exact or erroneous output.

IV. Power Dissipation of QCA structures

The power dissipation in QCA circuits has been studied extensively in [7]. The Power in QCA circuits are maintained by the Kink energy and adiabatic clocking Phases [4]. There is an electrostatic interaction between the neighboring cells in QCA for cells i and j can be given by Equation 3.

$$E_{ij} = \frac{1}{4\pi\varepsilon_o\varepsilon_r}\frac{q_i q_j}{|R_i - R_j|} \qquad \text{Eq. (3)}$$

The Kink energy is given by the difference between the same and opposite polarization of the neighboring cells in QCA which is given by equation 4.

$$E^k_{ij} = E_{ij(OppositePolarization)} - E_{ij(SamePolarization)} \qquad \text{Eq. (4)}$$

The kink energy (E_K), tunneling energy of an electrons (γ) and the Polarization (P) is related by the Hamiltonian equation of a QCA Cell i which is given by Equation 5

$$H_i = \sum_j \begin{bmatrix} -\frac{1}{2}P_j E_{ij} & -\gamma_i \\ -\gamma_i & +\frac{1}{2}P_j E_{ij} \end{bmatrix} \qquad \text{Eq. (5)}$$

Hence the total polarization of ‘cell-i' depends in the stationary states of overall cells given by

Equation 6. $H_i|\psi\rangle = E_i|\psi\rangle$ Eq. (6)

Hence it is necessary to study the energy dissipation in QCA circuits. The QCADesigner-E [11] tool is utilized for evaluate the energy dissipation as shown in Fig 10.

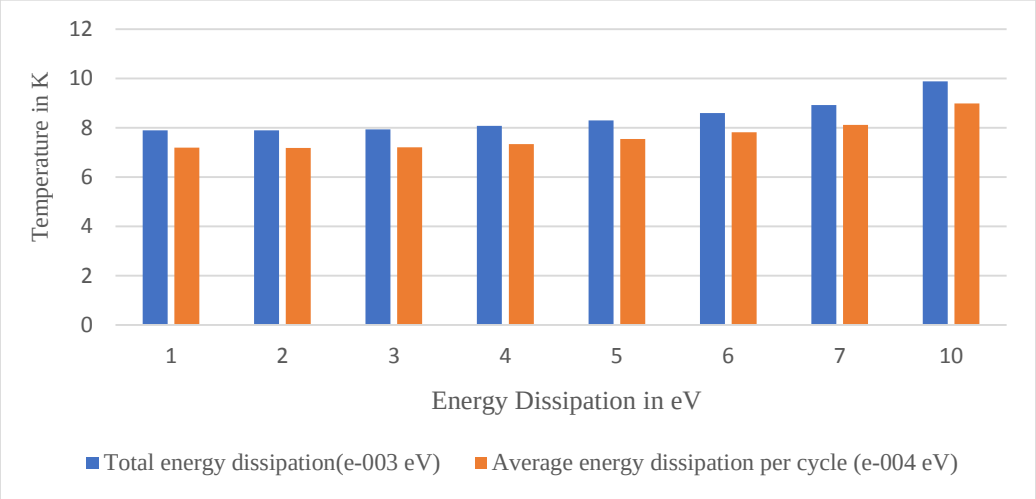

Fig 10 Temperature Vs Energy Dissipation of a Five Input Majority Voter

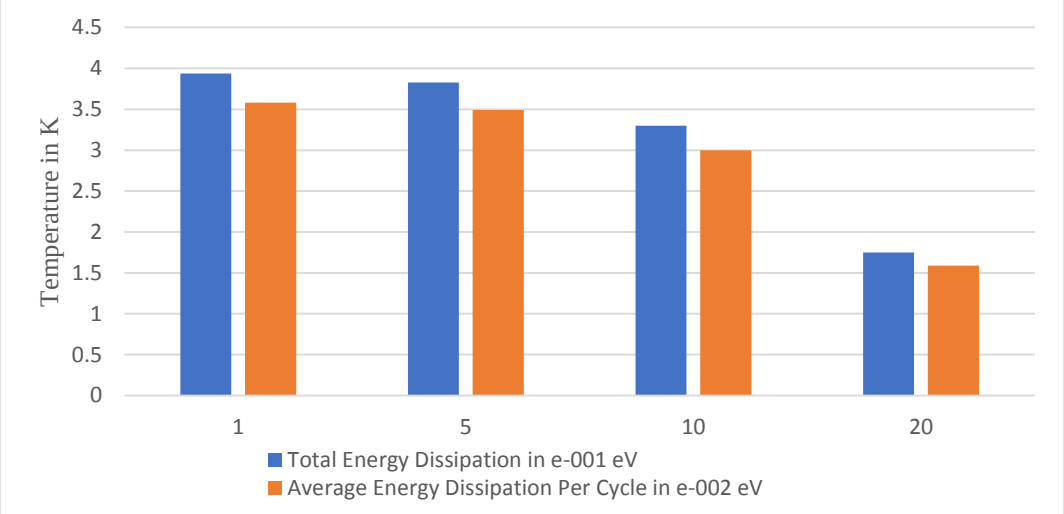

Fig 11 Temperature Vs Energy Dissipation of a 3 to 8 Decoder [6]

From the Figure 10 and 11, it is observed that the energy dissipation varies as there increase in temperature. Hence the probability of occurrence of exact output is dependent on the power in the circuit which is altered by the temperature on which the QCA circuits is operated.

V. Conclusion

Thus, the present research focusses on the reliability of obtaining a correct output of a 3 to 8 decoder by using Bayesian network with circuit level analysis using Macromodel. The circuits are checked for the reliability through the outcomes occurred in each state of Directed acrylic Graph. The temperature stability and the power dissipation are studied and the maximum likelihood occurrence of the output is analyzed for the high input 3 to 8 decoder using Power dissipation analysis. The work can be further extended for high input majority voter QCA architectures for thermal stability, reliability and energy dissipation.

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