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Methods of Fractography Analysis Applicable to Understand the Solid-State Lighting Chip Crack Origin

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ABSTRACT

This paper reported an example of a light-emitting diode (LED) failure with vertical chip crack, proposed an evidence method to identify the crack initiation zone and interpreted the fracture feature to understand the crack direction. Fractography by Secondary Electron Microscopy (SEM) imaging was employed to visualize the fracture features. It has demonstrated the century-old method used to study fracture surface of metallic and ceramic materials is still presently relevant in the age of semiconductor.

Keyword: Fractography, Crack, Die Attach, Void.

1. INTRODUCTION

Fractography has been widely applied to study the macroscopic appearance of fracture surfaces involving metallic materials starting in the eighteenth centuries [1] and brittle materials example ceramic and glass in late nineteenth centuries [2]. However, analogue technology only applicable to solid state materials [3,4]. Fracture topographical information after an event of cracks could lead to localization of the crack initiation zone.

The present paper describes some of the results obtained during the failure analysis of non-conformance chips. The results shown in Figure 1 consist of microscale fractography features such as twist hackles (*th*), velocity hackles (*vh*), Wallner line (*w*), striation (*s*), and arrest line (*a*) [5]. The driving force applied on the chip could be direct or indirect. When the driving force is direct contact with a chip, it is commonly associated with the crack initiation zone such as crack branching from chip sidewall effect of mechanical separating a wafer, cratering on bond pad effect of ultrasonic wire bonding or chip edge chip-off as a result of improper chip placement. When the driving force has indirect contact with a chip, the macroscopic level analysis of the package before resin decapsulation is crucial to observe for mechanical features such as scratches or indentations on the package. This is vital to prevent the misinterpretation of the fracture mechanism.

The motivation of this paper is to demonstrate the approach of decapsulation and the application of fractography analysis as a new perspective in understanding light-emitting diode (LED) chip crack origin. Today's LED chips by aspect ratio to silicon integrated circuit (IC) are at least five times smaller. LED chips are encapsulated in a cup-liked pre-moulded silicone to enhance light reflection instead of dark epoxy resin encapsulant with a flat-based for IC. The non-destructive techniques used to analyse silicon IC chip crack are x-ray microscopy and Scanning Acoustic Microscopy (SAM) [6,7]. The LED small aspect ratio is a challenge in x-ray microscopy handling and finding crack lines, losing a customer return sample is the last thing we are expecting. SAM is transmitting and detecting reflected acoustic waves; this works well in flat based IC packaging

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but creating many noises for the detector when dealing with a cup-liked shape LED packaging. Without both non-destructive techniques in LED failure analysis disposal, the analyst could not know the crack location. Figure 2 shows the proposed failure analysis flow developed for exposing and preserving the topographical fracture features in LED chips.

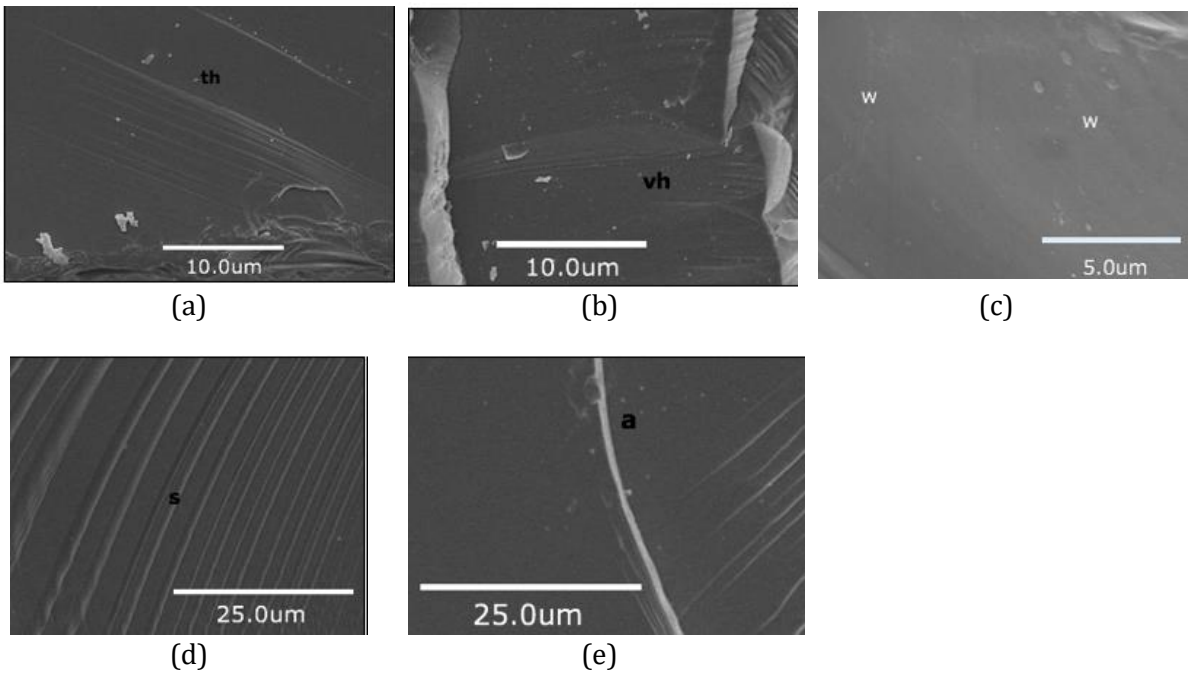

Figure 1. Example of microscale fractography features where (a) twist hackles (*th*), (b) velocity hackles (*vh*), (c) Wallner line (*w*), (d) striation (*s*), and (e) arrest line (*a*).

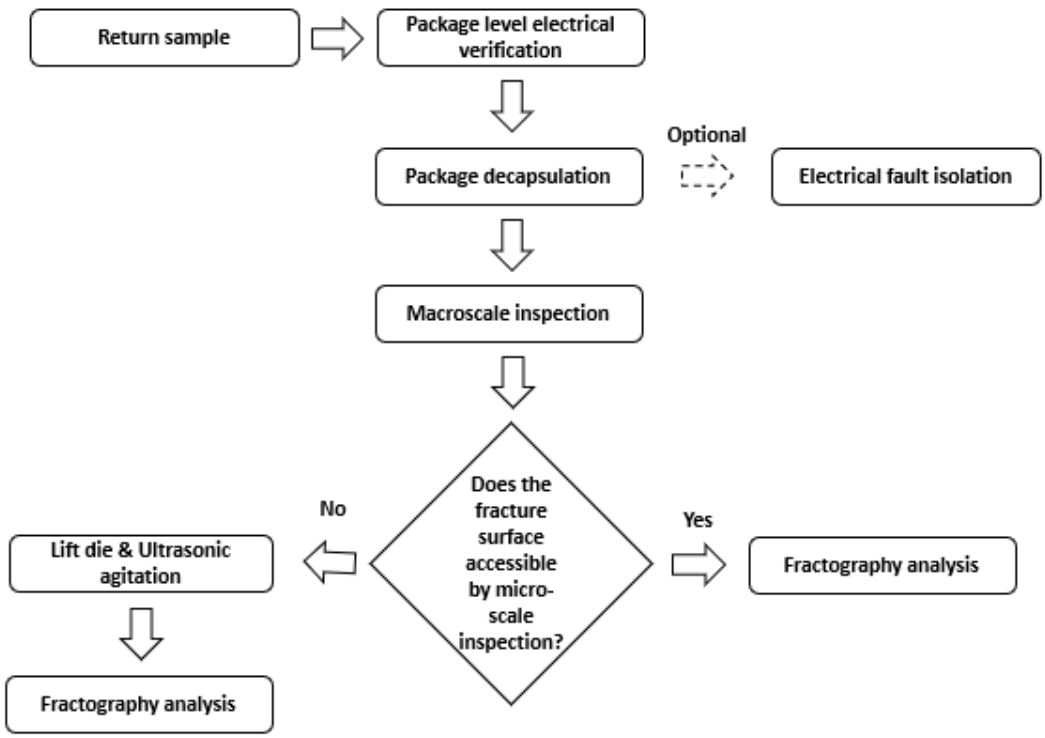

Figure 2. Fractography failure analysis flow.

2. METHODS

2.1 Decapsulation

A sample that was returned from customer often comes in the form of assembled package and seldomly comes in bare chip or chip on foil with a frame. The assembled package is suitable for exposure by chemical decapsulation but never by mechanical decapsulation which could further influence the crack system.

The optoelectronic device generally encapsulated in the silicone-epoxy copolymer; its solvent is "Dynasolve 711" [8] which is compatible with most metals, Teflon, polyethene, and polypropylene. "Dynasolve 711" [8] solvent is not compatible with nylon, polyvinyl chloride (PVC), urethane, titanium, and aluminium. The same solvent "Dynasolve 711" [8] could use for lifting epoxy glued chip with longer duration. The chemical composition of this solvent is propylene glycol monomethyl, methyl alcohol, and potassium hydroxide.

The sample cleaning and preservation after decapsulation is significant to avoid chemical or mechanical damages. Figure 3 shows the image from a high power microscope of common chemical damage that has resulted in incomplete removal or dilution of the etchant residual. After chemical etching, a sample is cleaned by a reducing agent (such as ethanol, propanol or acetone) in an ultrasonic bath before dried in 55°C oven. When working with the lifted die, tweezer cannot be used while handling the die in order to avoid further crack artefact. As an alternative to tweezer, a soft tip suction is recommended.

Figure 3. An optical representation of chemical damage on metallization if chemical residual not wholly removed.

2.2 Macroscale Inspection

Fractography analysis begins at a macroscopic level using an optical microscope to examine the primary crack and secondary crack branch off. Figure 4 shows that macroscopic examination helps narrow down the area that needed inspection in order to find the crack initiation zone.

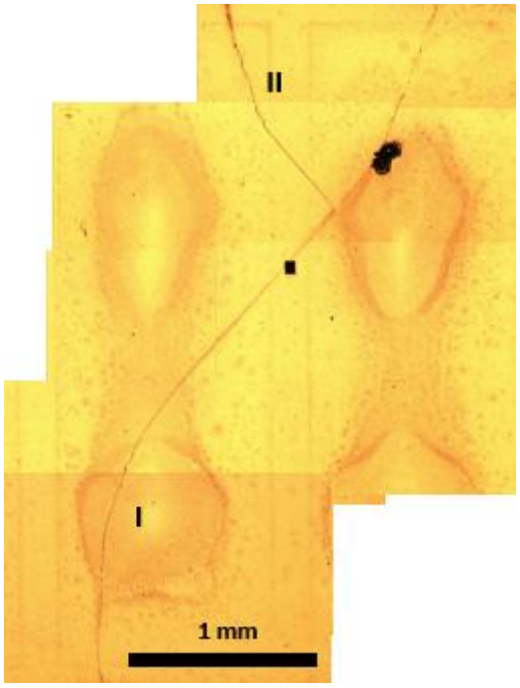

Figure 4. Macroscopic inspection of the sample reveals primary crack (line I) occurs before secondary crack (line II). The focus area to look for crack initiation zone will be on the surface of line I.

2.3 Ultrasonic Agitation

Once the chip was lifted from its substrate, the fracture surface might remain firmly intact. Ultrasonic agitation is one of the low costs and low complexity technique by applying bubbles implosion to expose the fractured surface and keeps it free from mechanical contact to avoid misinterpretation of the fracture event. The ultrasonic agitation medium utilizing distilled water is readily available in the semiconductor industry. Ultrasonic agitation is a suitable technique for minimum one fracture surface in contact with chip edge. By capturing some macroscale images or SEM micrograph for easy identification of the primary fractured surface when sample proceeds for microscale analysis are easier to locate those smaller fracture features. The other fractured surface(s) induced by bubbles implosion is a secondary fracture surface which is not the area of interest. The primary and secondary fracture surface can be differentiated by referring to the fractography feature-arrest line.

2.4 Micro-Sectioning

When chip crack further away from edges, there is an innovative method of using micro-sectioning which was shared by FK in 2013 [9] in order to expose the crack fragment. Figure 5 shows the formation of a micrograph of a cheesecake-like isolated island. Thereby, the crack fragment further away from edge could be either exposed by a short duration of ultrasonic agitation or exposed by welding to a micro-manipulator for lifting.

Figure 5. A cheesecake-like isolated island creates by the focus-ion beam (FIB). It reprinted with permission from [9] and not according to the scale for protecting proprietary information.

3. APPLICATION IN FAILURE ANALYSIS

3.1 Quality of Epoxy Die Attach and Its Relationship to Vertical Die Crack

[100] silicon substrate of a LED was epoxy die attached to copper leadframe. Epoxy interconnecting die attached material consists of a resin-hardener matrix, silver filler, adhesion promoter, anti-bleeding agent, etc. forming an electrical and thermally conductive adhesive. The conductive adhesive is thermal cure based on its thermal profile; during thermal cure process diluents or solvents are evaporated turning the conductive adhesive into a dense network of conductive filler particles. The thermal curing steps have further induced the different thermal expansion coefficient on a silicon substrate, and copper leadframe which is the main factor for residual stresses, therefore, controlling of adhesive void fraction and uniform thickness as output variables are essential [10].

Figure 6 is an example of a poor die attached in the form of a void fraction causes a different interface thermal resistance in the LED package. Package-to-board lead-free solder reflow process temperature could range from 250°C – 300°C which is sufficient to create a thermal cyclic event on every single unit.

Figure 6 and 7 are failure cases when the indirect contact mechanisms are the upward motion of the ejector pin couple with a downward movement of the clapper misalignment flexing the package to the extent encapsulated chip develops complete horizontal crack propagation.

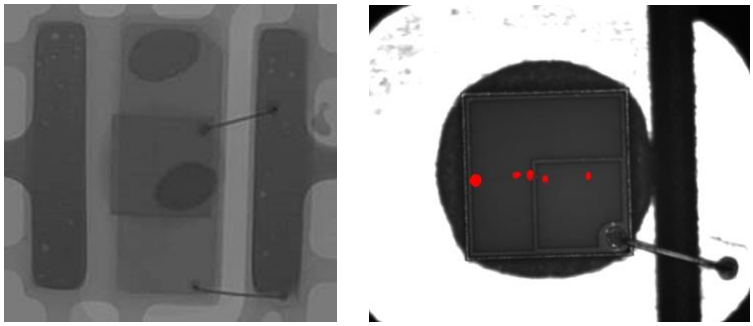

Figure 6. [Left] The x-ray radiograph top view shown insufficient epoxy adhesive underneath the chip. [Right] Photon emission microscope (PEM) is an electrical fault isolation technique used to review hot spots.

The hot spot pattern does suggest a crack line causing some electrical leakages. Package decapsulation has confirmed a vertical chip crack. Both pictures are not according to the scale for protecting proprietary information.

During the thermal cyclic event, the thermal stress and thermal strain of the chip with higher void fraction could result in chip crack. It is evident with the reducing of void fraction in the die attach layer will lead to an improvement of thermal resistance, which is an effective method to enhance the thermal and mechanical performance of high-power LED [11]. The thermal resistance of a material is related to thermal conductivity coefficient, R_{th} of material, heat transfer area and thickness of material as shown in Equation (1).

$$R_{th} = \frac{L}{KA} \tag{1}$$

Where,

K = thermal conductivity coefficient
L = thickness of the die attach material
A = heat transfer area

The micrograph in Figure 7 shows the crack front accelerated the mirror (m) region and merged into an area known as Wallner lines (w) as the result of tensile stress oscillation.

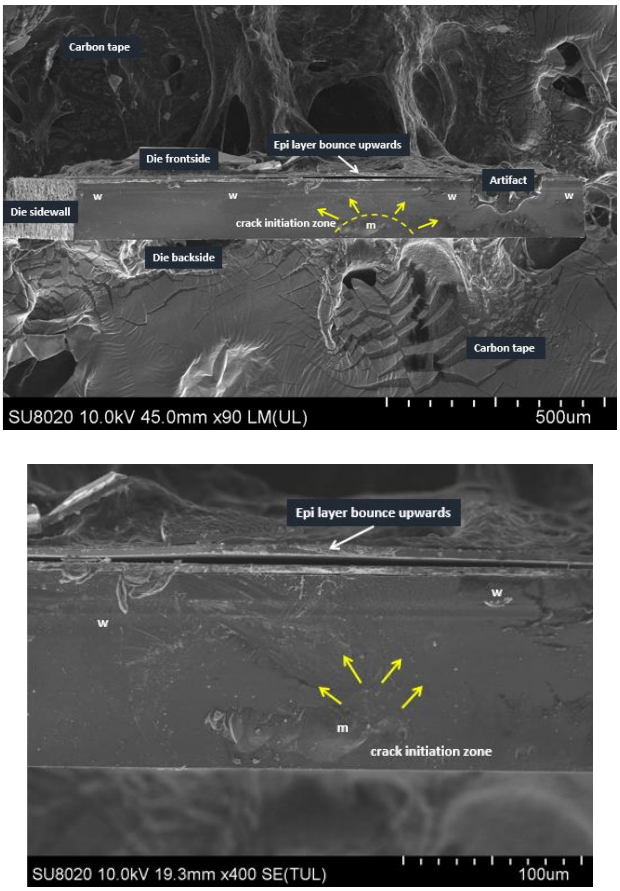

Figure 7. [Left] Micrograph shows the fracture chip vertically stick using carbon tape onto the scanning electron microscope (SEM) stud thereby the fracture surface is better to expose for viewing. [Right] Micrograph is a close up on fracture feature of a mirror (m) and Wallner (w) lines; LED epitaxial layer observed bouncing upwards.

The Wallner lines (w) are representative of the successive crack front shape which indicate the direction of crack propagation. The spacing between Wallner lines (w) is wider if the tensile stress at the crack front is higher due to higher stress. Besides, the velocity of the crack front also increases and the sonic wavefront intersects the crack front at larger distance intervals. Wallner lines (w) do not appear when a crack propagates at extremely slow or breakneck speeds. At extremely low speeds, the sonic waves generated are relatively weak and diminish behind the crack front. At extremely high speeds the fracture surface is too rough for Wallner lines (w) to be visible [12, 13].

All of the indicators to provide an evidence-based chip crack analysis were consolidated. A large solder void underneath a chip could increase thermal stress and strain to the chip [10]. The fracture feature-mirror (m) has placed the crack initiation zone within the silicon substrate, not from the chip backside. Figure 8 shows an example of crack initiation from chip backside. Another fracture feature – Wallner lines (w) interval indicate the crack propagating from the crack initiation zone within the silicon substrate towards the chip frontside. The force generated by the chip cracks has resulted in epi layer delaminated and bounce upwards.

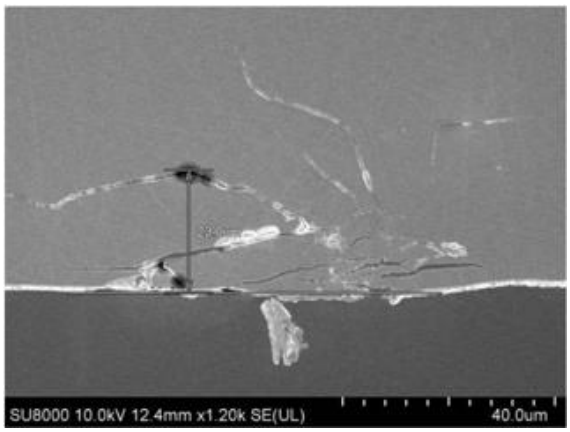

Figure 8. An example of the crack initiation from chip backside cross-sectional view.

4. CONCLUSIONS

Through the given an example, the crack-related quality topic in present days semiconductor could be analysed with evidence base like any other semiconductor failure topics. It has demonstrated the century-old method used to study fracture surface of metallic and ceramic materials still presently relevant in the age of semiconductor.

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