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A Simplified Surface Potential Based Current Model for Gate-All-Around Carbon Nanotube Field Effect Transistor (GAA-CNFET)

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ABSTRACT

This paper presents a simple surface-potential based drain current (I_d) model for gate-all-around carbon nanotube field effect transistor (GAA-CNFET). The model captures a number of features which include ballistic transport, first subband minima, chirality and non-existence of fringing and screening effect due to its geometry. Further, the effect of chirality on subthreshold swing (SS), current on/off ratio ($I_{ON/OFF}$) and transconductance (g_m) is studied by extracting these parameters from drain current variation. It is observed that there exists a trade-off between the parameters for different chiral vector CNTs. As chirality increases, transconductance and subthreshold slope increases while current on/off ratio reduces. To confirm the validity of proposed model, virtually fabricated GAA-CNFET device performance was simulated and compared with the calculated values. The variation is also compared with the experimental result of actually fabricated device. The close match between calculated, simulated and experimental results confirms the validity of the proposed model.

Keywords: Carbon nanotube, carbon nanotube field effect transistor (CNFET), chirality, device modeling, Subband

1. INTRODUCTION

Carbon nanotube field effect transistor (CNFET) is considered as one of the preferable candidates to complement silicon (Si)-based metal-oxide semiconductor (MOS) devices [1-3]. One of the key factors that restrict further scaling of Si MOS devices is the short channel effects (SCE), which degrades the performance of the device in terms of high power consumption during turning off the device [4-6]. The advantages of carbon nanotubes (CNTs) include energy-efficient computation because of their high carrier velocity and near-ballistic carrier transport property [7-9]. Moreover, due to very thin structure of CNT, the gate control of the CNFETs is superior and this makes it capable to overcome the SCE even in the sub-10 nm technology node [10-11]. In recent years, a lot of advancement has taken by various research groups [12-16] and addressed key challenges in the CNFET technology.

In order to understand the performance of CNFET, it is utmost important to study the performance of the fabricate device based on the optimization obtained using simulation results. However, it is also important to assess the results and understand the physics behind transport mechanism based on an analytical model. Various approaches have been used for analyzing the performance of CNFET. Some extensively employed methods include;

Nonequilibrium Green's function (NEGF) formalism, Landauer formula [17-18], virtual source approach and optimized geometry approach [11-12, 19]. However, these methods are computationally expensive, have limited scope and based on parameter extraction.

In this paper, a simplified model for gate-all-around CNFET (GAA-CNFET) is proposed which is based on the dependency of current on the surface potential of CNT. The main features of this model include:

(i) The model is based on the ballistic transport of charge carriers in channel.

(ii) Screening and fringing effects are neglected as GAA structure is free from sharp edges.

(iii) The effect of chirality of CNT on the performance of the device.

(iv) The model has been verified against the simulated results and published experimental data.

This paper is organized as follows: analytical expressions, theory behind the development of this model and parameter extraction are described in Section 2. Section 3 explains the results and discussion obtained from analytical model and simulations. It also describes the effect of chirality on drain current (I_d) and finally the conclusion of this study is given in section 4.

2. THEORY AND MODEL

To understand the working of CNFET, many approaches have been used. J. luo et al. [19] proposed a compact model for multichannel CNFET. This model has semiempirical approach for CNFET. The screening effect is considered for modelling due to multichannel CNT. C-S Lee et al. [11] presented a data calibrated model which is based on virtual source approach. A. Deyasi et al. [27] described a current model for CNFET using NEGF approach. They have analysed drain current, subthreshold swing and quantum capacitance for GAA-CNFET, however this method is computationally expensive. In the proposed model, screening and fringing effects are neglected due to GAA structure with single wall CNT in channel. The performance of CNFET is mainly dependent upon I_d which is controlled by gate. The effectiveness of gate control further depends on various other parameters which include; type of gate dielectric material, chirality and diameter of CNT [28]. Other electrical parameters which effect the device performance are gate-to-source voltage (V_{gs}) and drain-to-source voltage (V_{ds}). For the choice of gate dielectric material, a systematic study was performed to select the best possible gate material for GAA-CNFET. It was found that lanthanum oxide (La_2O_3) and hafnium oxide (HfO_2) are the best gate dielectric material to be used for GAA-CNFET [20]. In order to compare our result with that of experimental one, it was assumed that gate dielectric is made up of HfO_2 and the structure considered for GAA-CNFET is shown in Figure 1.

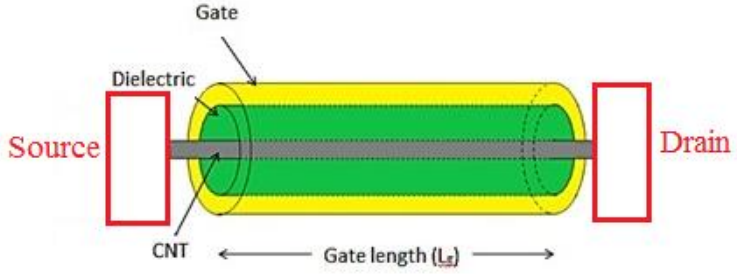


Figure1. Gate-all-around CNFET device structure used in current model.

The procedure used for computing the I_d includes the consideration of the energy of each subband and the associated probability of occupation in these subbands. The intrinsic CNT contains two types of charge carriers, one with positive velocities and other with negative velocities, hence the total I_d in channel can be written as:

$$I_d = \frac{2q}{h} \times \left[\int F(E, E_F - qV_{gs}) - \int F(E, E_F - qV_{ds}) \right] dE \quad (1)$$

where h is Planck's constant, $F(\,)$ is the Fermi function, $E_F - qV_{gs}$ and $E_F - qV_{ds}$ are the Fermi levels in the source and drain contacts, respectively. Considering zero source voltage and integrating from energy level $E_{cb} - qV_{CNT}$ to infinity, we can represent Eq. (1) as:

$$I_d = \frac{2q}{h} \times \int_{E_{cb} - qV_{CNT}}^{\infty} \left[F(E, E_F - qV_g) - F(E, E_F - qV_d) \right] dE \quad (2)$$

The degeneracy occurs due to two or more than two subbands having same energy level, therefore the additional factor of 2 is included in Eq. (2), hence solving Eq. (2) gives;

$$I_d = \frac{4qkT}{h} \times \left[\ln\left\{1 + \exp\left(\frac{qV_{CNT} - qV_g - \Delta_1}{kT} \right)\right\} - \ln\left\{1 + \exp\left(\frac{qV_{CNT} - qV_d - \Delta_1}{kT} \right)\right\} \right] \quad (3)$$

where, V_{CNT} is the surface potential and Δ_1 is the first subband minima. V_{CNT} can be represented by following empirical relationship [21]

$$V_{CNT} = \begin{cases} V_g & \text{for } V_g < \Delta_1 \\ V_g + \alpha(V_g - \Delta_1) & \text{for } V_g > \Delta_1 \end{cases} \quad (4)$$

where, $\Delta_1 = \frac{E_g}{2q}$ (first subband minima) and α is the slope of the curve which is calculated by following equation [22]

$$\alpha = \alpha_0 + \alpha_1 V_g + \alpha_2 V_g^2 \quad (5)$$

where α_0, α_1 and α_2 are empirical parameters which can be calculated by matrix method.

$$\begin{bmatrix} \alpha' \\ \alpha'' \\ \alpha''' \end{bmatrix} = \begin{bmatrix} 1 & V_g' & V_g'^2 \\ 1 & V_g'' & V_g''^2 \\ 1 & V_g''' & V_g'''^2 \end{bmatrix} \begin{bmatrix} \alpha_0 \\ \alpha_1 \\ \alpha_2 \end{bmatrix} \quad (6)$$

In order to calculate α_0, α_1 and α_2, we analysed the behaviour of GAA-CNFET for various gate voltages (V_g). Though the values of these empirical parameters are available for planar structure [21], but we have calculated these parameters for GAA structure by using the output characteristics of GAA-CNFET. Figure 2 shows the output characteristic of GAA-CNFET for 30

nm channel length [23]. The empirical parameters α', α'' and α''' in Eq. (6) are the slope of drain current corresponding to V_g of 0.5 V, 0.75 V and 1.0 V, respectively. The value of α_0, α_1 and α_2 obtained are 1, -0.05625 V^{-1} and 1.175 V^{-2}, respectively.

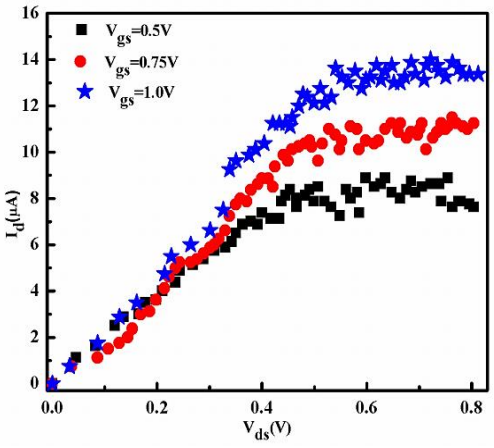


Figure 2. Experimental I_d-V_{ds} characteristics of GAA-CNFET. Experimental results Ref [23].

The first subband minima is the half of the energy band gap therefore Eq. (3) can be rewritten as:

$$I_d = \frac{4qkT}{h} \times \left[\ln \left\{ \frac{1+\exp\left(\frac{qV_{CNT} - qV_g - \Delta_1}{kT} \right)}{1+\exp\left(\frac{qV_{CNT} - qV_d - \Delta_1}{kT} \right)} \right\} \right] \tag{7}$$

So, the final drain current equation obtained depends on surface potential of CNT, chirality of CNT, gate voltage and drain voltage.

3. RESULTS AND DISCUSSION

In order to analyze the performance of GAA-CNFET, CNT (19, 0) has been considered because the diameter of this CNT is 1.49 nm which is same as that of the CNT diameter of fabricated GAA-CNFET. the I_d has been calculated using Eq (7) and compare it with fabricated result. In order to use the value of Δ_1, we need the energy band gap (E_g) of CNT (19, 0). For this we analyzed the energy band diagram of CNT (19, 0) using Atomistic QuantumATK tool. Figure 3 shows the band structure of CNT (19, 0) which gives the energy band gap (E_g) of 0.5005 eV. The conduction minima and valance band maxima are 0.2489 eV and -0.2516 eV, respectively.

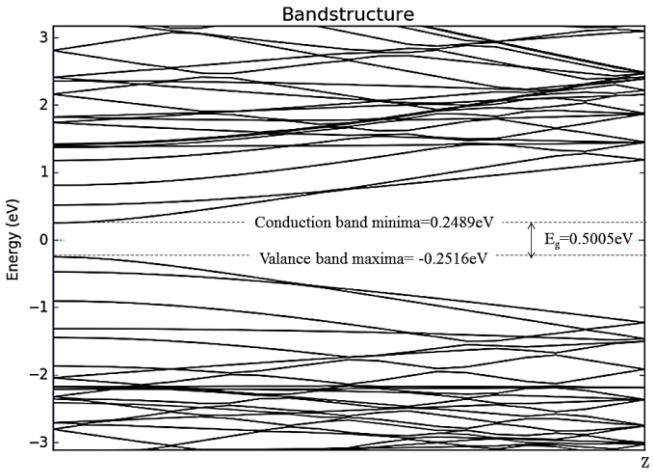
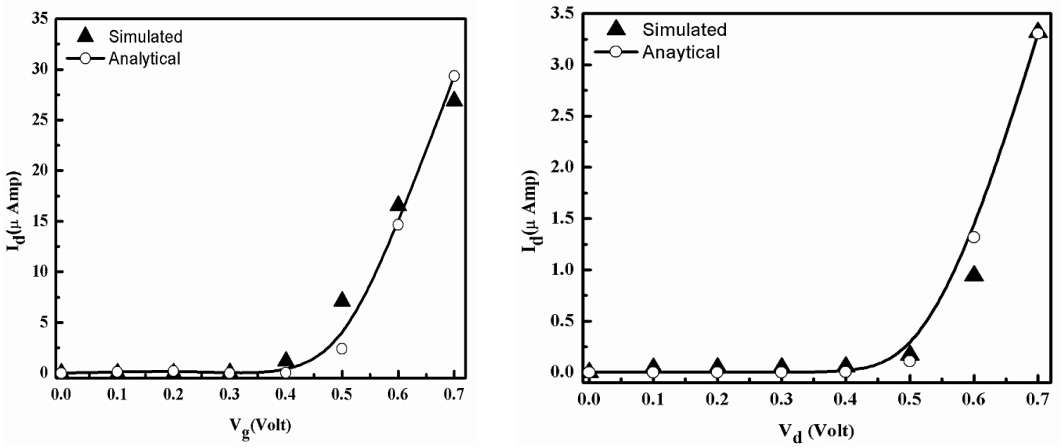


Figure 3. Energy band structure for CNT (19, 0)

In order to confirm the validity of the current model, GAA-CNFET is virtually fabricated and its performance was analyzed using Technology Computer-aided Design (TCAD) simulator. Figure 4 shows the transfer and output characteristics plotted using analytical model and using simulation. It is observed from Figure 4 (a), that as V_g increases beyond 0.4 V, a steep rise in the drain current is observed. This is attributed from the fact that minimum 0.4 V is required for the carrier to overcome the potential barrier at the channel end. This trend shows the excellent match for the calculated value of drain current and the simulated results. Figure 4 (b) shows the output characteristic of GAA-CNFET. It is observed that analytical values are approximately same as the simulated result. The solid lines in Figure 4 are the best fitting curve of calculated values based on analytical model.



(a) (b)

Figure 4. Comparison between the calculated and simulated (a) transfer and (b) output characteristics of GAA-CNFET at V_d and V_g of 0.3 V, respectively.

Chirality (*n*, *m*) of CNT depends on its diameter and hence on its energy band gap which further also affects surface potential of CNT (V_{CNT}). This indicate that the I_d of CNFET will also depend on the chirality (*n*, *m*) of CNT. The diameter (*d*) and energy band gap (E_g) of CNT are given by [24]:

$$d = \frac{\sqrt{3}a_{c-c}}{\pi}\sqrt{n^2 + nm + m^2} \tag{8}$$

and

$$E_g = \frac{2a_{c-c}t}{d} = \frac{0.852}{d(nm)}(eV) \tag{9}$$

where, t is the nearest-neighbour hopping parameter and $a_{c\text{-}c}$ is the carbon-carbon bond length. Table 1 shows the calculated and simulated values of diameter and energy band gap of zigzag type CNT (n,0) [26]. A folded graphene sheet along with one of two chiral vectors at chiral angle of 0˚ angle defines as zigzag CNT (n, 0). It is observed that as chirality increases, diameter of CNT increases but its energy band gap decreases. This inverse proportional trend of bandgap of CNT with its diameter is also observed from Kataura plot [25]. It is also observed that diameter and energy band gap values from simulation and calculation are close to each other.

Table 1 Diameter and energy band gap of different CNTs

CNT	Diameter (nm)		Energy Band Gap (eV)	
	Calculated	Simulated	Calculated	Simulated
(10, 0)	0.7830	0.7829	1.0880	1.0534
(13, 0)	1.0179	1.0178	0.8369	0.8178
(16, 0)	1.2528	1.2526	0.6800	0.6668
(19, 0)	1.4877	1.4875	0.5726	0.5633
(25, 0)	1.9576	1.9572	0.4352	0.4299

In order to study the effect of chirality on the performance of GAA-CNFET, the device was virtually fabricated using TCAD simulator and its performance was studied. Figure 5 (a) shows the transfer characteristics of GAA-CNFET using different CNTs (CNT (10, 0), CNT (13,0), CNT (16, 0), CNT (19, 0) and CNT (25, 0)). It is observed from the plot that for all types of CNTs, drain current increases sharply with increase in gate voltage beyond 0.4 V. It can also be depicted from the graph that as chirality of CNT increases, drain current also increases. Typically, the drain current for CNT (25, 0) and CNT (10, 0) are 33.483 µA and 27.2743 µA at V_g = 0.7 V, respectively. Although there is high output drain current for CNT (25, 0), but it has less gate control after the V_g of 0.2 V. Figure 5 (b) shows the output characteristics of GAA-CNFET using different chiral CNTs. It is observed from the plot that as drain voltage increases, CNT (10, 0) and CNT (13, 0) does not show any significant drain current. However, for other CNTs drain current increases with increase in drain voltage. The trend shows that as chiral vector increases drain current also increases.

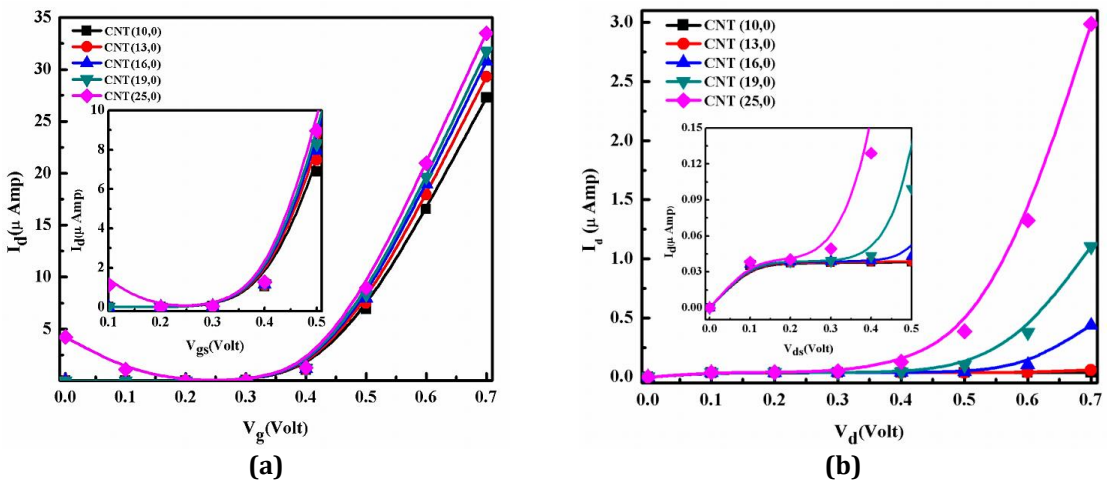


Figure 5. Effect of chirality on GAA- CNFET (a) transfer characteristics (b) output characteristics at V_g and V_d of 0.3 V, respectively.

In order to further analyze the characteristics of GAA-CNFET, effect of chirality on subthreshold slope, $I_{ON/OFF}$ ratio and transconductance is also studied using the device characteristics and parameters are extracted using Data Graph Digitizer software tool. In FET devices, high on/off ratio, subthreshold slope and transconductance are required for reducing the leakage current and high switching speed. These parameters with their values are listed in Table 2. It is clear from the table that there exists a tradeoff between the parameters for a given chiral CNT. For example, there is high $I_{ON/OFF}$ ratio and less subthreshold slope for CNT (10, 0) and CNT (13, 0), however for these CNTs, device shows less transconductance value. CNFET with CNT (25, 0) has low $I_{ON/OFF}$ ratio because of less gate control which leads to high subthreshold slope. For CNT (16, 0), CNFET has moderate current on/off ratio and subthreshold slope and CNFET with CNT (19, 0) has high transconductance, so both CNTs (16, 0) and (19, 0) are suitable for GAA-CNFET.

Table 2 Characteristic parameters of CNFET

CNT	Subthreshold Slope (mV/dec)	I_{ON}/I_{OFF} Ratio ($\times 10^6$)	Transconductance (μS)
(10, 0)	69.96	70.406	58.2621
(13, 0)	75.32	77.823	63.7227
(16, 0)	79.24	24.693	67.9316
(19, 0)	81.87	0.6509	71.0808
(25, 0)	86.55	0.0115	76.8234

In order to check the validity of this simplified surface potential-based current model, we have compared the results obtained from simulation and analytical model with experimental results available in literature for fabricated GAA-CNFET [23]. Figure 6 shows the comparison of the transfer characteristics between experimental, simulation and analytical model for GAA-CNFET. The variation between the drain current versus gate voltage shows similar trend with the fabricated device. The small variation between experimental and analytical results may be

attributed due to the fact that in fabricated device, an adhesion layer of ~1-nm AlO_xN_y is also used with 8 nm HfO_2 as a gate dielectric. Therefore, the close match between results confirms the validity of the proposed model.

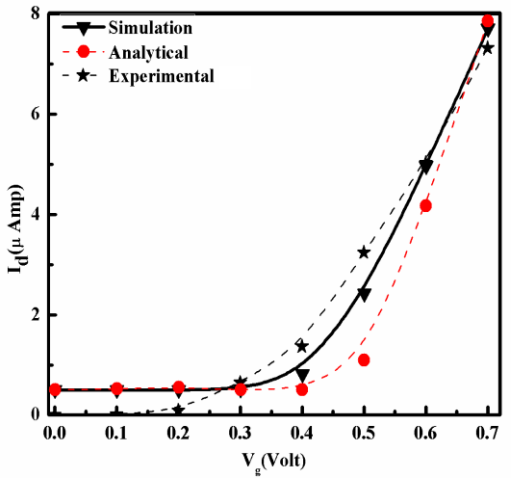


Figure 6. Comparison between analytical results with simulation and experimental results [23]

4. CONCLUSION

We have proposed a surface-potential based model to investigate the performance of the GAA-CNFET in this paper. In the simplified surface-potential based model, the drain current depends on the surface potential of CNT. This model is based on the ballistic transportation of the charge carriers and neglect the screening and fringing effects. We also studied the effect of chirality on the device performance and it was found that CNT (16, 0) and (19, 0) shows average on/off ratio and high subthreshold slope and transconductance as compared to other chiral CNTs. Later, to validate the proposed model, results were compared with the experimental results of fabricated device using CNT (16, 0) as channel in CNFET. The close match between these two results confirms the validity of proposed model.

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