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Fabrication of nano and micrometer structures using electron beam and optical mixed lithography process

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Abstract

In this paper, the fabricated pattern of nanometer and micrometer structures created with electron beam lithography (EBL) and optical lithography on silicon on insulator (SOI) material are presented. The resist used to demonstrate this EBL pattern creation is ma-N 2403 which is a negative tone photoresist series, while positive resist PR1-2000A is used to transform photomask design using optical lithography. Three different patterns structures are fabricated on each sample namely alignment mark, silicon nanowire and metal pad. The JEOL scanning electron microscopy (SEM) has been modified to integrate with RAITH software to be used for electron beam lithography. Nano-scaled nanowires were first patterned by EBL and formed by ICP etching followed by micro-sized contact pads were defined by photolithography process. The approach describe in this paper is a mix-and-match techniques using both conventional photolithography and advanced nanolithography, making use of an alignment strategy.

Keywords: Nanowires; Electron beam lithography; Device characteristics.
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1. Introduction

Lithography is the process of transferring patterns from one medium (mask) to another medium (wafer). Lithography can be classified into conventional lithography and unconventional lithography such as UV-lithography and e-beam lithography respectively. There were many intensive research topics on scaling down the size of devices. Although photolithography gives the best throughput, it is not achievable to pattern smaller than ~30nm features because of its resolution limit [1]. As an example, even the refractive optical lithography is anticipated to reach its wavelength limit, beyond which significant issues arise in terms of availability of light sources, masks and the need for new photoresist materials [2]. Other lithography techniques, there are emerging technologies including EUV lithography, Electron and Ion beam projection lithography to offer higher resolution as a solution for replacing photolithography technology [3]. Even though other techniques are good for smaller patterns, EBL is optimized for device studies because of its speed and reliable reproducibility, and also is suitable for the features of silicon nanowires. Many microdevices and systems required fabrication of microstructure over large areas in combination with smaller nanostructured regions on the same sample surface [4]. Large area micrometer to nanometer scale features are most efficiently defined by optical lithography whereas EBL method is used

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for fabricated nanostructures scale [5, 6]. In this work, we present combined electron beam lithography and optical lithography to define both micrometer and nanometer scale features. The exposure process to fabricate nanowire is carried out by an in-house modified electron beam writing system using JOEL JSM 6460LA SEM integrated with ELPHY Quantum pattern generator. The process flow for the electron beam lithography and optical lithography is illustrated in Figure 1 which is adopted from [7].

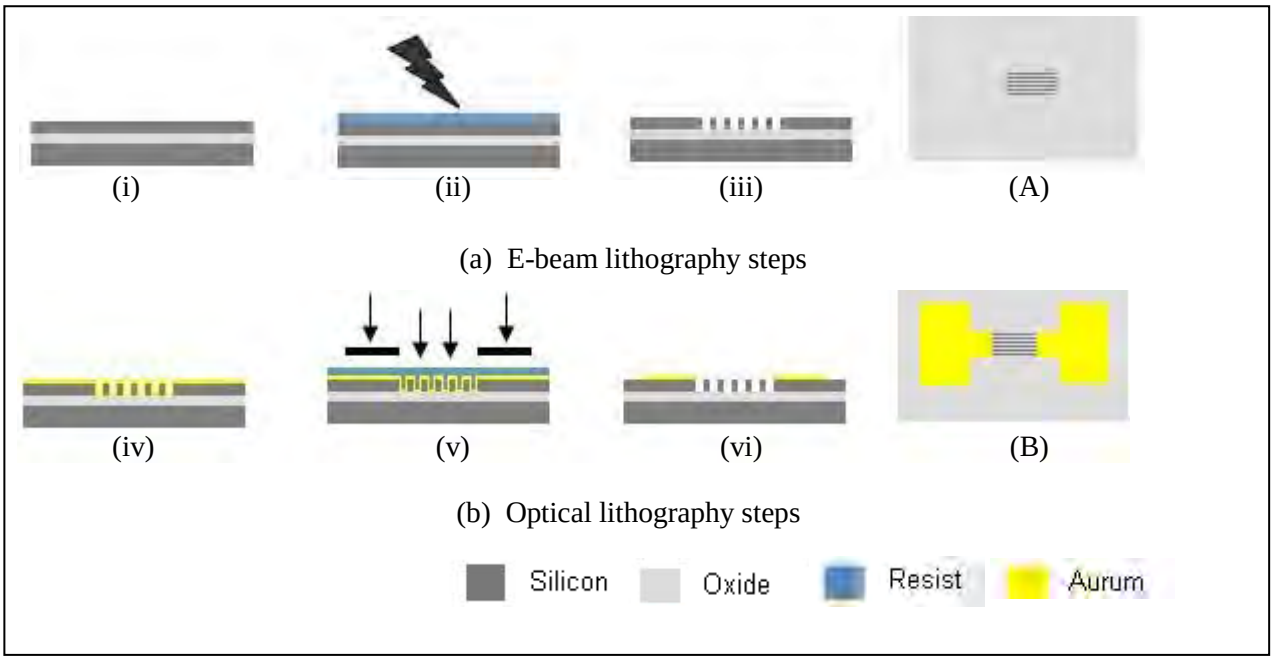

Fig. 1: Experimental scheme of electron beam lithography coupled with optical lithography. (i) a cleaned SOI sample (ii) coated sample is exposed using EBL (iii) after development process and resist strip (A) top view of nanowire fabricated using EBL (iv) electron beam evaporation of Au onto the sample surface (v) optical lithography exposure (vi) wet etching of a deposited Au layer using the resist as mask (B) top view of aligned source and drain pad.

2. Experimental Details

The 4 inch (100 mm in diameter) p-type silicon on insulator (SOI) wafer which initially had a 160 nm silicon layer on a 200nm buffered-oxide (BOX) insulating layer with resistivity 1-20 Ωcm was used as the starting material. The wafer was first cut into 1.5 cm x 1.5 cm samples for ease characterization using scanning electron microscope (SEM) and atomic force microscope (AFM). Standard cleaning procedure using RCA1, BOE, and RCA 2 was used to remove organic and inorganic contaminant on the samples surface. Then, the samples were baked using conduction hot plate at 200°C for 5 min to remove residual water and cooled down in room temperature in 60 min. The general scheme of this work is shown in Figure 1. Before patterning for the nanowire using electron beam lithography, the etch alignment marks were defined by optical lithography followed by reactive ion etch (RIE). Subsequent to alignment marks formation, negative tone ma-N 2403 resists were spun (spinner model WS-400B-GNPP/UTE/10K) at 3000 rpm for 30 s. The coated sample was prebaked on the hot plate (JB-TEK Honeywall) at 90°C for 60 s. After cooled down to room temperature, the resist film was exposed using electron beam lithography system as given in Table 1. After exposed, the sample was developed in ma-D 532 solution for 30 s followed by rinse in DI water for 5 min. The exposure times to perform this nanometer scale features are short to due to the high electron sensitivity of ma-N 2403.

Table 1: Exposure Parameters

Acc. Voltage	20kV
Working Area	800 µm x 800 µm
Magnification	100 X
Beam Current	0.075 nA
Area Dose	100 µC/cm^2
Area step size	10 pixels

Then, the micrometer size features were defined by optical lithography using positive photo resist. This method is used for fabricated electrode pad which is started with resist coating on the Au layer, followed by prebake on the hot plate at 90°C for 60 s, expose at Mask aligner and UV radiator for 8s and development in resist developer RD6. Lastly, the pattern creation and visual inspection take place for the patterned profile using High Power Microscope and SEM (JEOL 6460).

2.1 Mask design

There are three masking steps that used in the present process namely alignment mark for mask 1, silicon nanowire for mask 2 and metal pad for mask 3. The alignment mark and metal pad were designed using AutoCAD. Nanowire pattern was designed using GDS II Editor Software. The masks were fabricated on the chrome mask as shown in Figure 2 (a) and it is used as the photo mask for optical lithography process. The nano pattern design using GDS II Editor Software as shown in Figure 2 (b) was used as the pattern creation during electron beam exposure.

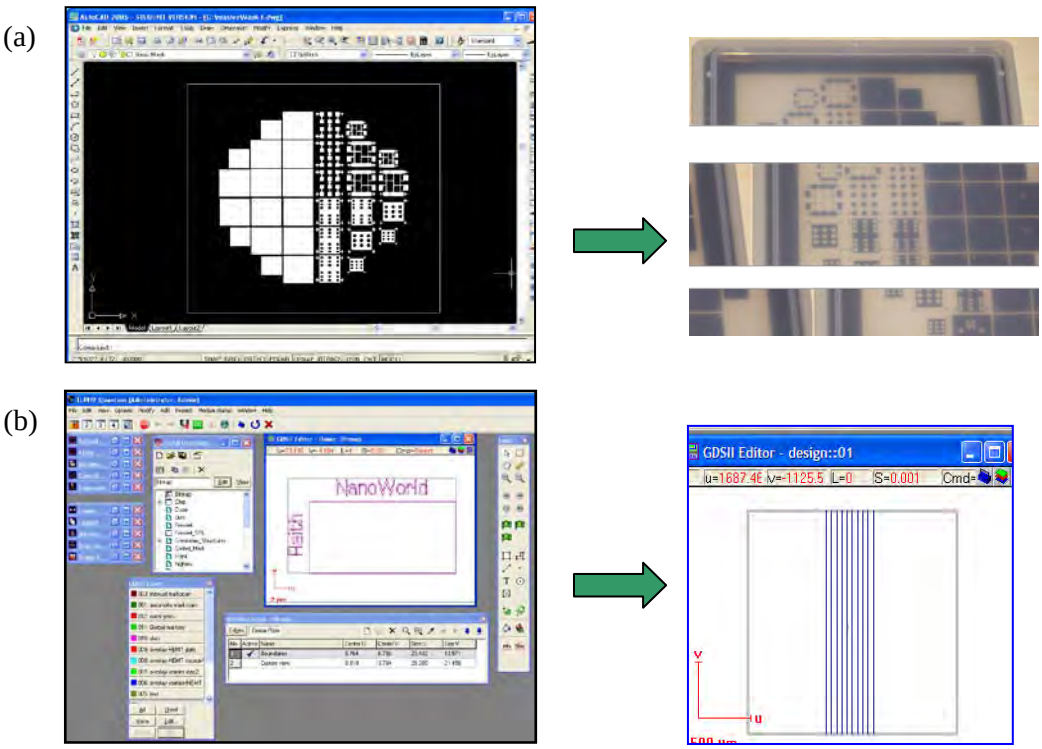

Fig. 2: (a) AutoCAD design fabricated on chrome mask (b) nanowire pattern design using GDS II Editor Software.

3. Results and discussion

This section presents the results of the experiments achieved. These include the fabrication of nanowire using electron beam lithography, the formation of alignment mark and metal pad via optical lithography, and the function of the alignment system.

3.1 Pattern fabricating using e-beam and optical lithography

Before patterning the nanowire via electron beam lithography, an array of cross-shaped alignment marks was etched in silicon substrate using the optical lithography process. These cross-shaped patterns served as the alignment keys to locate the nanowire during e-beam lithography process and simplified the alignment process during the exposure different pattern using optical lithography. Starting with plain p-type SOI wafer, a 300 nm oxide layer was deposited on top of silicon surface by using PECVD for providing masking layer in KOH etching of silicon. For this work, a 30% KOH at 80°C was found the optimum for silicon etching and minimum damage to oxide hard mask. The alignment marks are patterned with standard optical lithography. Permanent alignment marks with ~1 micron depth was fabricated and inspects using Ambios Technology XP – 1 Stylus Profiler as can see in Figure 3 (c). The alignment mark mask dimension is illustrated in Figure 3 (a) and Figure 3 (b) shows the SEM image of the fabricated alignment mark on the sample surface.

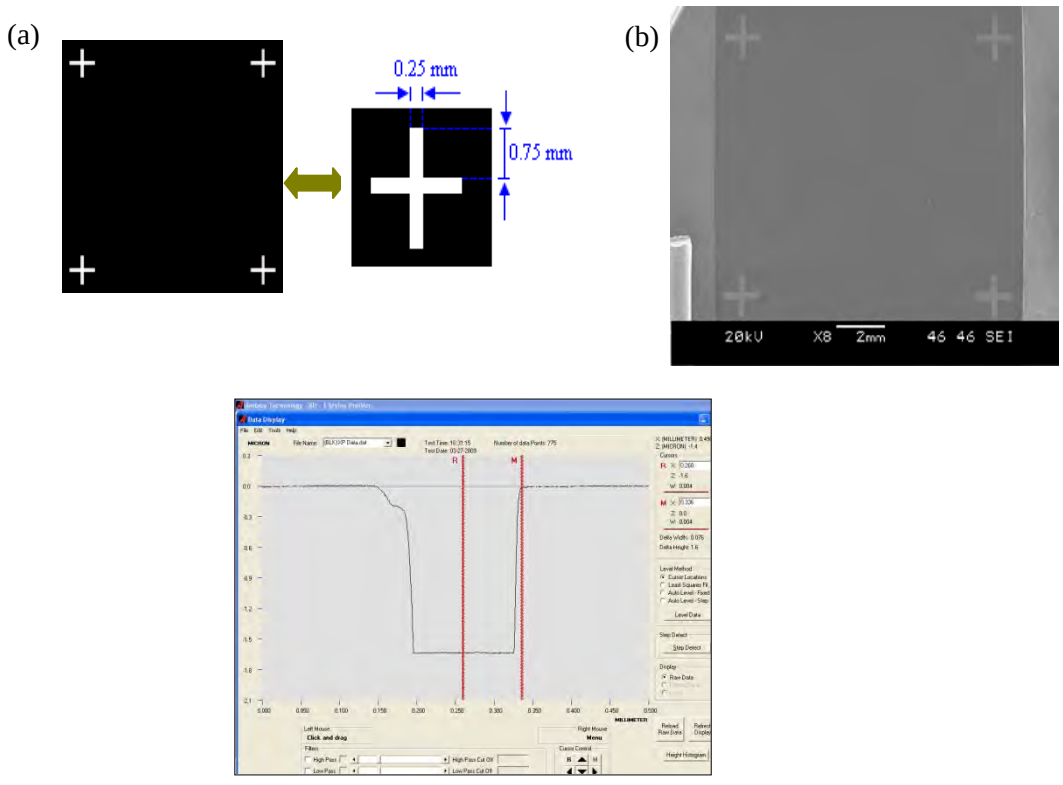

Fig. 3: Sequence of alignment mark formation is shown. (a) Schematic drawing of mask 1. (b) SEM image of fabricated mask 1. (c) Stylus profiler scan of the etch alignment mark.

Subsequently, the silicon nanowire were defined by electron beam lithography and formed by ICP etching process. RAITH –ELPHY Quantum software was used to design the

nanowires pattern. Figure 4 (a) shows the design consisting of 800 µm x 800 µm frame of working area. Nanowire patterns varied from 40nm to 100nm width with a gap of around 3µm separating each other. These patterns were designed by considering the effects of the resolution of the lithography in which the optimum resolution of ma-N 2403 negative resist is 50 nm and minimum area step size of version 4.0 Raith software EBL is 40 nm [8]. To expose pattern design on the resist surface, EBL system is first set up as shown in Table 1. Figure 4 (b) shows the SEM micrograph of 5000 X magnification. After resist development and etching process, 90 nm width of nanowire with separately by 3 µm gaps were successfully fabricated. The actual design of the nanowire pattern was 50nm with a gap 3 µm. There is about ~40nm difference between the size of nanowire design and experimental fabricated sized of nanowire structure. The SEM micrograph of 80 nm silicon nanowire as given in Figure 4 (c) at 50 000X magnification. The figure clearly indicates the quality of silicon nanowires structure with good uniformity, high resolution and line edge smoothness.

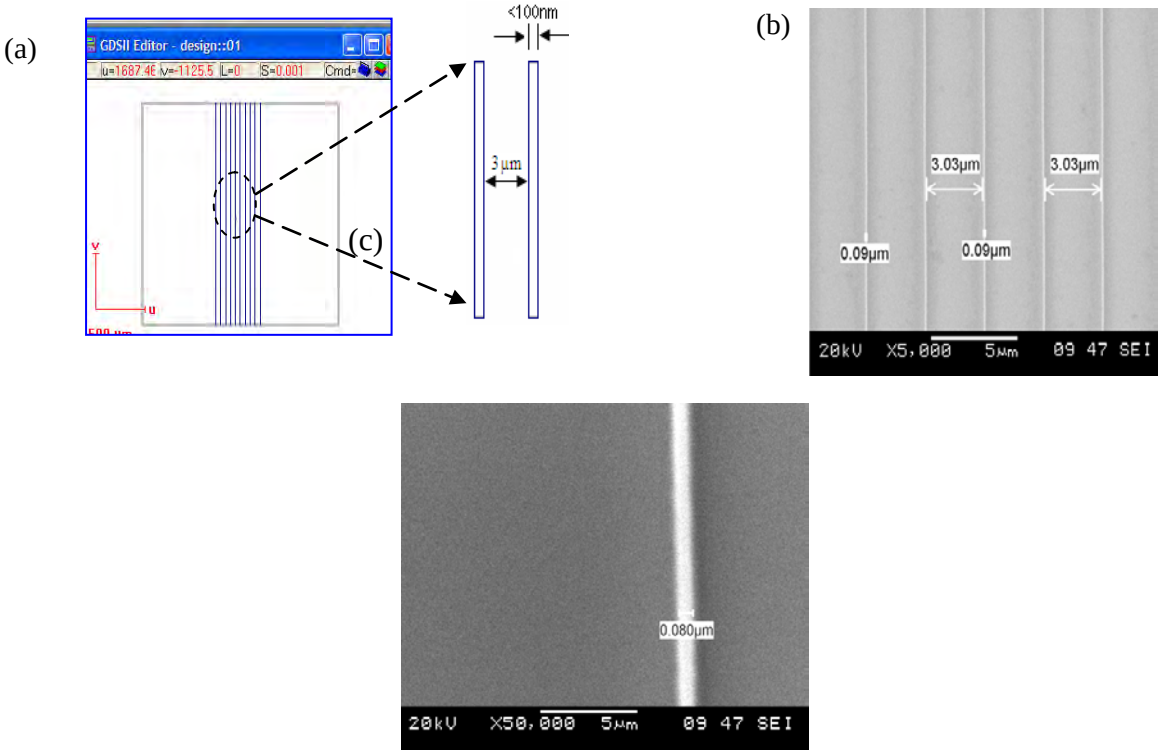

Fig. 4: Sequence of nanowire formation. (a) Nanowire pattern design using GDS II Editor Software. (b) SEM image of fabricated nanowire structure. (c) SEM image of 80 nm nanowire observed by 50K magnification.

Figure 5 (a) is a schematic drawing of mask 3 with the dimension for source and drain pad formation. Figure 5 (b) shows the SEM imaging of mask 3 pattern transfers on the sample surface using optical lithography. Based on the design, there are nine gaps between the electrodes pads, means there are nine SiNW FET will fabricated on each sample. Figure 5 (c) shows the SEM image of the end of two probing electrodes fabricated using optical lithography on an oxide surface. The electrodes pad is separated by a gap of 150 µm. The source and drain pads were formed by e-beam evaporator of 10 nm of Ti and followed by 50 nm of Au. Aqua regia was used to etch the Au layer and Ti layer in room temperature. This solution is formed by freshly mixing between HNO_3 and HCL with volumetric ratio of 1:3 respectively.

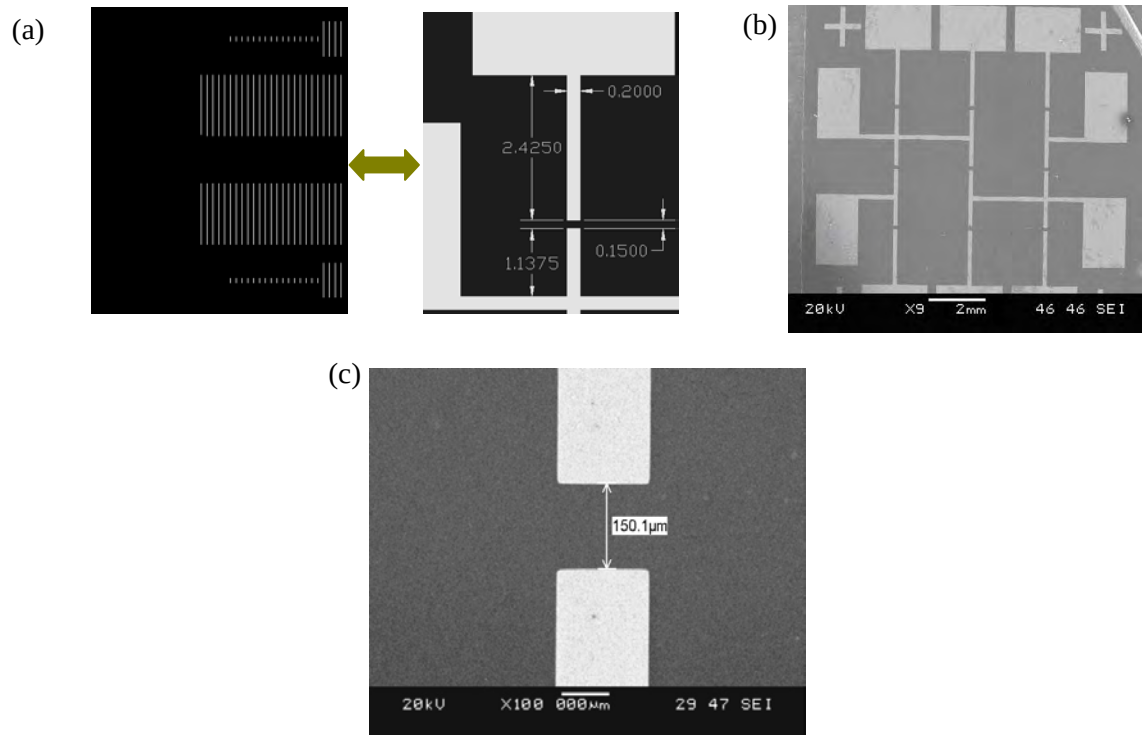

Fig. 5: Sequence of electrode pad formation is shown. (a) Schematic drawing of mask 3 (b) SEM image of fabricated mask 3. (c) SEM image of the gap between the electrodes without nanowire formation is presented.

3.2 Alignment System

In direct-write electron beam lithography, the smaller size pattern must be accurately aligned with existing structures on the sample. The accuracy of the coordinate has a significant influence on the functionality and performance of the device. Several challenges have to be overcome for placing nano scale structure at the accurate coordinate in this separate patterning of the large and small features in two different lithography steps. A reasonable approach to overcoming this problem is to fabricate the micro-sized of alignment mark structure by optical lithography as the first step and followed by nanowire formation using electron beam lithography. The purpose building or fabricating these structures first is to form the reference point to locate the accurate coordinate during nanowire pattern design exposure and easily for mask alignment during photolithography process.

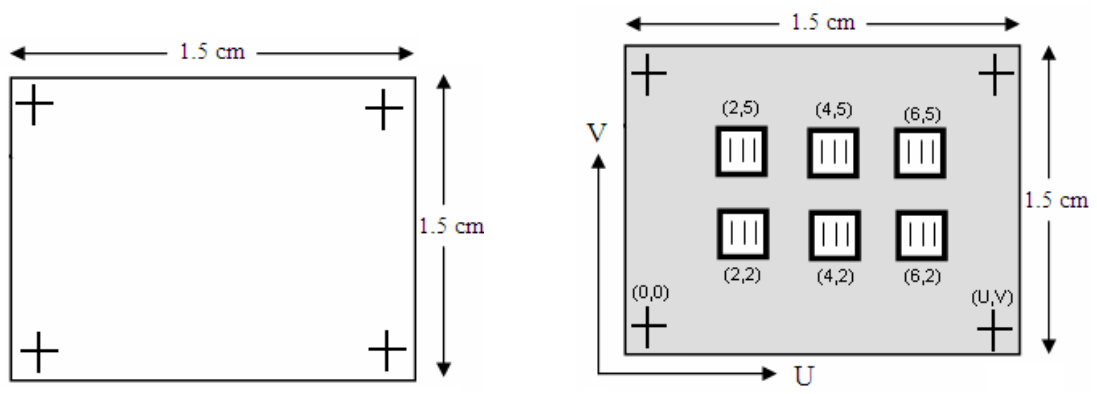

Fig. 6: The illustration of (a) alignment mark structures fabricated via optical lithography process (b) U-V coordinate system in EBL.

After completing the nanowire design using GDS II editor, the U-V coordinate system is used in EBL system as shown in Figure 6 (b). U-axis is for horizontal and the V-axis is for vertical. Design coordinate system is defined by design layout and the movement of the beam. This step is very important to know the location of pattern exposed on the sample and easily to find the structures during SEM imaging. In addition, the fabricated alignment mark via optical lithography as the first steps as shown in Figure 6 (a) has been the reference point (0,0) for the e-beam exposure coordinate. This coordinate system is helpful in design process to form the precise location of nanowire structure for the next metal pad fabrication step. Thus, the precise coordinate has been measured by analyzing the placement accuracy of numerous structures exposed on samples.

Figure 7 shows three alignment steps which influence three different results. The portion of nanowire is observed using High Power Microscope with magnification 100X. The blue color of the alignment illustration as shown in Figure 7 (a) are represent the fabricated alignment mark structure on the sample while the red color of alignment mark as shown in Figure 7 (b) is represent the designed of mask 2 in the chrome mask. This step was done during the alignment steps using optical lithography system as. Figure 7 (c) shows the perfect coordinate to locate the 800nm length of the five lines nanowire structures which connected between the two contact pads. To control the patterning result, pictures were taken at different stages from the developed resist patterns to make sure no breaking part in the middle of nanowire during the developing time. Before exposure the pad structure using optical lithography, make sure to meet the alignment mark of sample to alignment of mask by control the θ-axis, X-axis and Y-axis of stage. In this mix and match lithography, the nanoscale fabrication must be aligned with larger components to produce the completed device. An important feature of the instrument is the alignment system which enables the electron beam lithography fabrication step to be aligned with nanometer accuracy with respect to the larger components in the device.

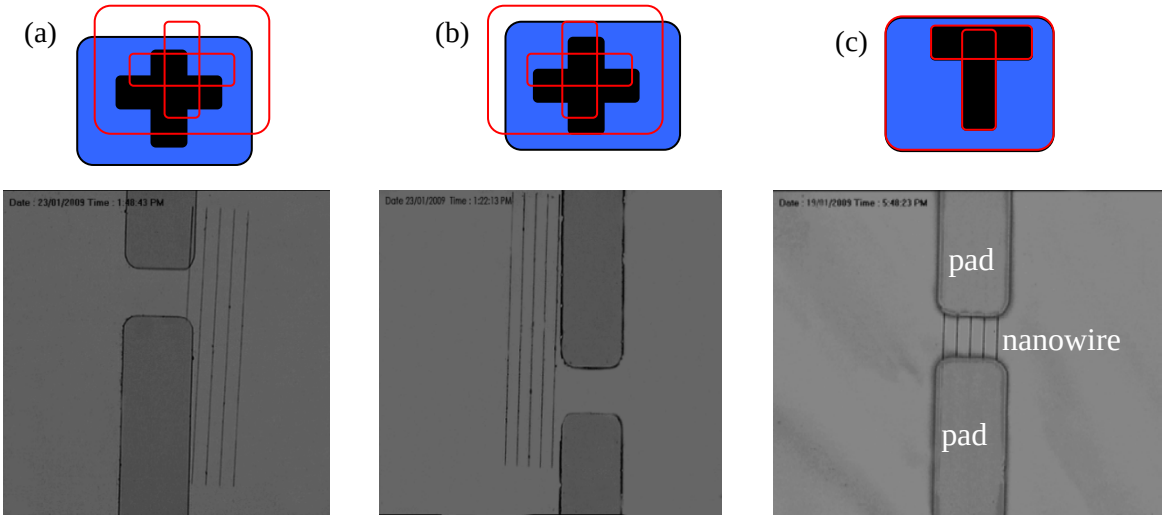

Fig. 7: (a) (b) and(c) HPM image observed the connected nanowire between the two electrode pads with different alignment steps.

3.3 Device characteristic

The transport properties of various semiconducting nanowires have demonstrated their potential for diverse electronics devices, such as for p-n diodes, field effect transistors, and switches [9,10]. Next, the characteristics of the fabricated Si structures were characterized electrically in air by measuring two terminal current-voltage characteristics. A typical I-V curve of a junction for 100nm of Si nanowire is shown in Figure 8, which shows a standard diode characteristics. Note that the response shown is a composite of several NWs under the Al electrode. The curve shows that this device had high resistance and tended to break down at lower voltages. In principal, according to Li et al. [11], the I-V characteristics of the SiNWs were linear, and the conductance generally scaled proportionally with the dimension of the wires. As shown by data points in Figure 9, indicating that good ohmic contact between the electrode pads and the SiNWs was formed. The current increases with the applied voltage, but no linear relationship in I-V behavior was observed. The slope of the I-V curve gradually increased with the voltage. The current through the wires with diameter 100nm is ~8.8 µA at 1.5 V forward bias, which is about 100 times larger than that reported by Harnack et al [12].

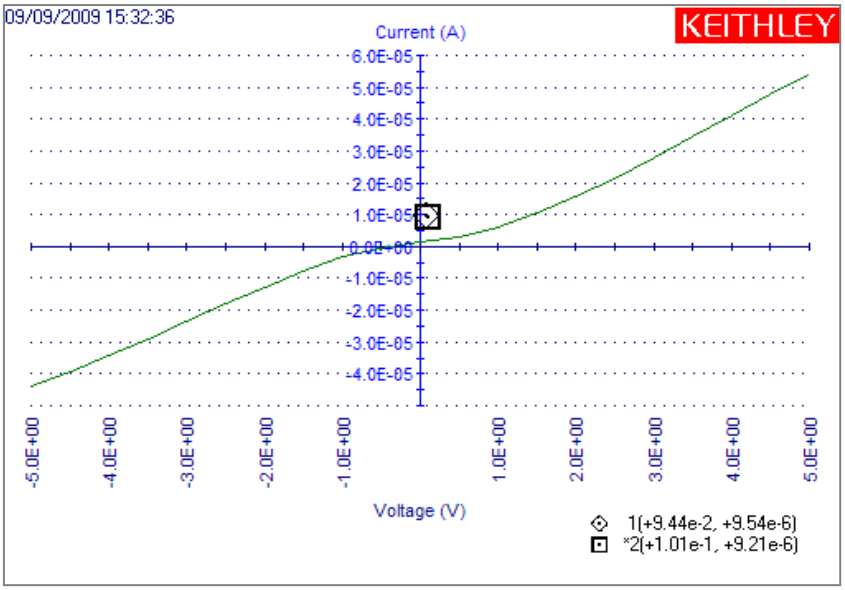

Fig. 8: The I-V characteristics of the devise in voltage range of -5 V to 5V

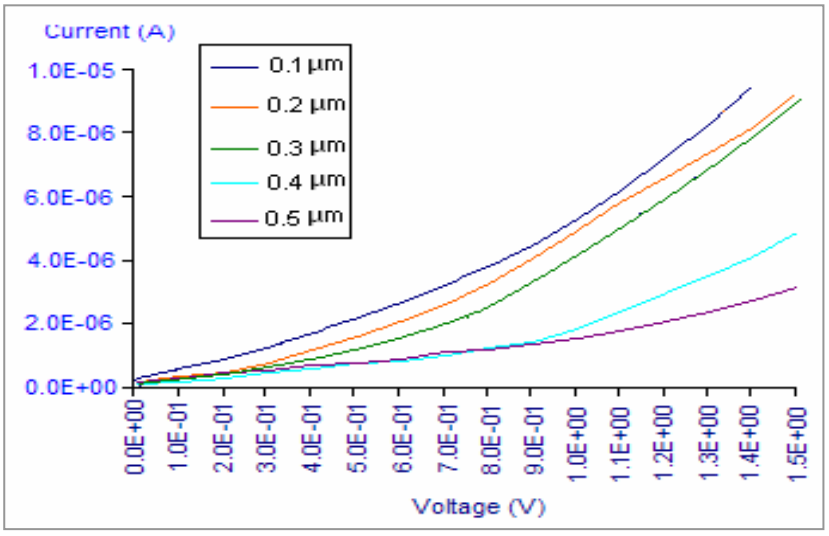

Fig. 9: I-V measurement through Si wires of various diameters showing diameter dependent electrical characteristics.

4. Conclusion

The fabrication of nanowire FET has limited number of factors to be considered. The two vitally important factors to consider during fabrication process were the nano-scaled sizes of nanowires must be below than 100 nm which patterned by electron beam lithography process and metal formation at precise locations on top of individual nanowire using optical lithography process. This step was very important in making reliable contact between the metal pads and the semiconductor nanowire. The nanowire with diameter of 80 nm and the precise coordinate of the metal pad was successfully fabricated and obtained in this work.

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