

Quantum mechanical direct leakage currents in a sub 10 nm mosfet: a rigorous modeling study

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Received 22 Jan. 2010; Revised 13 Jan. 2011; Accepted 1 Feb. 2011

Abstract

In this paper, we have developed a rigorous model for the quantum mechanical source to drain electron/hole tunneling in sub 10nm nanometer scale metal-oxide-semiconductor field effect transistor (MOSFETs). Inversion layer quantization, band-gap narrowing, drain induced barrier lowering (DIBL) and variable doping at source and channel have been included in the developed model. Results predict that the source to drain tunneling results in an increase of leakage currents in sub 10 nm MOSFETs and hence cannot be ignored. The results match closely with the numerical results already reported in literature proving the accuracy of the model.

Keywords: QME, WKB, Inversion layer quantization, tunneling

PACS: 85.35.-p, 85.40.Bh, 73.40.-c, 73.63.Rt.

1. Introduction

The scaling of a MOSFET into sub 10nm region is major challenge today due to severe leakage current occurring in MOSFETs. As per the International Technology Roadmap for Semiconductors (ITRS) [1], in 2016, the MOSFET gate length will reach 10nm region. The development in sub 10nm-level MOSFETs has also been reported in [2, 3]. The problems in down scaling have shifted the research from the traditional MOSFET to non conventional devices as reported in [4, 5]. The alternatives also suffer from disadvantages such as integration of these components with the existing silicon technology and packaging issues. The conventional CMOS technology for the microelectronic applications still dominates majority of the electronics industry. So, there is still a large scope of continuing with the existing MOSFET scaling to sub 10nm region. If we continue scaling the MOS technology to sub 10nm level, major limiting factor is the source to drain direct tunneling current density that increases the sub threshold current. This increases the static power dissipation in the MOSFET. If downscaling has to continue to sub 10nm scale, suitable MOSFET models are required to be incorporated in SPICE simulators.

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2. Physics and modeling of electron/hole tunneling in a sub 10 nm region

Electrons/holes tunnel from the source to drain through the substrate. The potential barrier height is reduced by gate and drain voltage. The existence of the source to channel barrier is lowered by DIBL. The modeling technique is based on first calculating the tunneling of electrons/holes from the source into the substrate and then from the substrate to the drain. A rigorous analysis is required to understand the source to drain tunneling by considering DIBL, inversion layer quantization process, band-gap narrowing and variable doping at source and channel. The existing work in sub 10nm MOSFETs quantum mechanical tunneling from source to drain has been carried out using numerical models [6, 7]. These models are quite complex and very difficult to be incorporated in the SPICE simulators. Another basic model has also been developed in [8]. But a detailed, physics based model is still desired to be developed which explains the source to drain direct tunneling process in detail.

In this paper, an improved DIBL influenced channel surface potential (V_m) has been modeled in detail and rigorously, detailed physics of inversion layer quantization has been given and the effect of DIBL on the substrate concentration has been empirically given in addition to the effects included in [8]. All these effects have been included in the basic tunneling current density equation modeled using Wentzel-Krammer-Brioullion (WKB) technique. Here, we use a MOSFET with variable doping near the source and different in the channel. The channel lengths taken in the study are of the order of 6nm, 5nm and 4 nm for study.

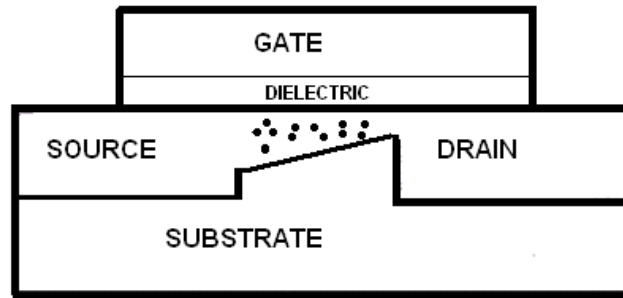


Fig 1: MOSFET showing direct tunneling

Modeling

The source to drain direct tunneling current density is a function of the width and height of the potential barrier between source and drain. Figure 1 shows the direct tunneling using the arrow from source to drain in inversion and in off conditions. The modeling has been done for electron tunneling only and can be extended to hole tunneling also. Using the WKB method [9], [10], the transmission probability $T(E)$ is obtained and is given by (1)

$$T(E) = \exp\left[-2\int_{x_1}^{x_2} |k(x)| dx\right] \quad (1)$$

$$k(x) = \left[2m_1 \frac{V(x) - Ex}{\hbar^2}\right]^{1/2}$$

The direct tunneling current density is given by (2) as reported in [9]

$$J_T = \left(\frac{4\pi m_l q}{h^3} \right) \int_0^V \left\{ \int_0^\infty [f_s(E) - f_D(E)] dE_y \right\} T(E) dE_x \quad (2)$$

Electron distribution at the drain/substrate interface = $f_D(E) = \left[1 + \frac{\exp(E - E_{fd})}{kT} \right]^{-1}$,

E_{fs} is fermi energy at the source, E_{fd} is fermi energy at the drain, E is the total energy of electrons, E_y is the energy in the direction perpendicular to tunneling. Using (1) and (2), the tunneling current density from source to drain can be evaluated.

$$J_T = \left(4\pi m_l q (kT)^2 / h^3 \right) \left(1 + \gamma_t kT / 2 \sqrt{V} \right) \exp(E_{fs}) \exp(-\gamma_t \sqrt{V}) \quad (3)$$

E_x = Energy of electron from source to drain, \hbar = Effective Planck's constant = $h/2\pi$, m_l = longitudinal electron mass = $0.916m_0$, Barrier Height (V) = $0.5(2V_{bi} + V_{ds}) - \phi_{sqm} - V_m$, $E_{fs} = 0.5 E_g - q\phi_f$, E_g = Silicon energy band-gap, ϕ_f = Fermi potential, V_{bi} = Built in potential at source or drain, V_{ds} = Drain to source voltage, V_m = Surface potential increase due to DIBL = $\gamma_t = 4\pi L(2m_l)^{1/2}/h$, ϕ_{sqm} = Quantum surface potential from [14]. L is the effective channel length.

Modeling of DIBL influenced surface potential (V_m)

Solving the Poisson's equation at the source/substrate interface and applying the boundary conditions, the potential variation as:

$$V_s(x) = V_{bi} (1 - x/W_1)^2 \quad (4)$$

Similarly, solving the Poisson's equation at the drain/substrate interface and applying the boundary conditions, the potential variation in the substrate as:

$$V_d(y) = (V_{bi} + V_{ds}) (1 - y/W_2)^2 \quad (5)$$

$y = L - x$, $W_1 = (2\epsilon_o\epsilon_{si}V_{bi}/qN_b)^{1/2}$ = depletion width at the source, $W_2 = \{2\epsilon_o\epsilon_{si}(V_{bi} + V_{ds})/qN_b\}^{1/2}$ = depletion width at the drain. N_b is the substrate concentration

Equating (4) and (5) and solving for x , we get,

$$x = (1 - R + RL/W_2) / (R/W_2 + 1/W_1); \quad R = \{(V_{bi} + V_{ds})/V_{bi}\}^{1/2} \quad (6)$$

Therefore, the minimum potential in the substrate is given by:

$$V_m = V_{bi} \{1 - (x/W_1)\}^2 \quad (7)$$

3. Inversion layer quantization physics and modeling

Another parameter that influences (3) is the inversion layer quantization in the channel of the sub 10nm MOSFET. Due to high doping in the substrate and ultra-thin gate oxide, very high vertical electrical fields are generated. These fields confine the movement of carriers in a narrow potential well existing between the surface potential distribution and the infinite oxide potential. The confined carriers are hence forced to occupy only discrete energy levels. The silicon energy band is composed of six equal energy lobes orienting towards six directions. Every energy lobe has two directions also. One is longitudinal and the other is the transverse direction. So, the electrons present in these two directions have masses $0.916m_0$ and $0.19m_0$ respectively. Let the Si/SiO₂ interface is towards (100) direction. So, the electrons in two lobes along the interface have mass $0.916m_0$ and in the other four lobes have transverse mass $0.19m_0$ along the Si/SiO₂ interface. So, combining these four lobes of transverse mass $0.19m_0$ are grouped together and the other two lobes are grouped together as shown in figure 2. When inversion layer quantization occurs, the electrons reside in lower energy valleys i.e. $0.916m_0$ mass. So, 90% of the electron population is in lower valley having longitudinal mass $0.916m_0$ and transverse mass $0.19m_0$. Also the lower valley is slightly above the conduction band edge of the silicon conduction band as also given by Heisenberg principle. This causes a significant decrease in the inversion carrier density at a Si/SiO₂ interface in MOSFETs as compared to that of the classical case. All the calculations done in this paper are based on the lower energy valley having longitudinal mass $0.916m_0$ and transverse mass $0.19m_0$.

The existing work in inversion layer quantization modeling is focused on calculating the inversion charge density using variation approach or triangular well approach as reported in [11]-[15]. The variation approach is used in this work to analytically and accurately model the inversion layer quantization. This is due to the high accuracy of this approach. Moreover, the equations are also solved explicitly bringing more accuracy in the results. Solving the Poisson equation in the inverted channel in a MOSFET, we get the total charge density, Q_s .

$$Q_s = -(2qN_a \varepsilon_{si} \varepsilon_0)^{1/2} \left[\varphi_s + V_t e^{-2\varphi_f/V_t} (e^{\varphi_s/V_t} - 1) \right]^{1/2} \quad (8)$$

q is electron charge, ε_{si} is silicon relative permittivity, ε_0 is permittivity of free space, φ_s is surface potential, φ_f is fermi potential, N_a is substrate concentration, and $V_t = kT/q$ is thermal voltage .

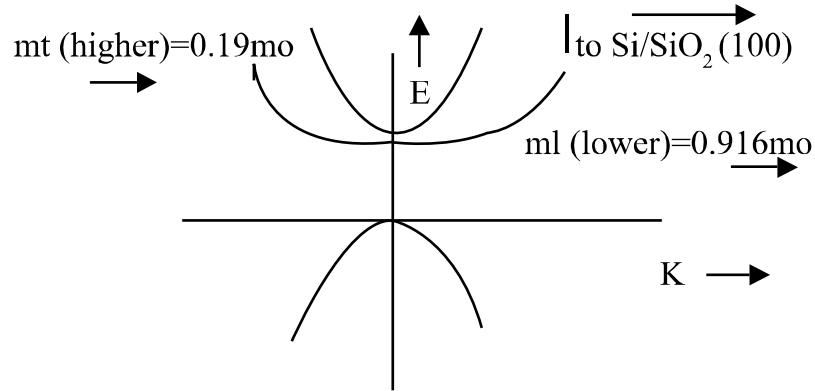


Fig. 2: E-k diagram showing inversion layer lower energy and upper energy and masses in the conduction band valleys.

Similarly, the depletion charge Q_b is approximated as

$$Q_b = - (2\epsilon_{si}\epsilon_0qN_a\phi_s)^{1/2} \tag{9}$$

Therefore, the inversion charge density Q_i is given by (8) and (9):

$$Q_{inv} = -\gamma C_{ox} \left\{ \left[\phi_s + \frac{kT}{q} \exp\left(\frac{q(\phi_s - 2\phi_f)}{kT}\right) \right]^{1/2} - (\phi_s)^{1/2} \right\} \tag{10}$$

γ is body effect parameter and C_{ox} is oxide capacitance (Fcm⁻²). The main problem with (3) is that the surface-potential has to be evaluated explicitly in all the regions of inversion and then only it can be solved. An explicit solution has been evaluated in [16]. The wave function solution of the Schrödinger's equation is given by using variation approach [11]:

$$\psi(x) = \frac{b^{3/2}x}{\sqrt{2}} \exp\left(\frac{-bx}{2}\right) \tag{11}$$

$$b = \left[\frac{48\pi^2 m_t q}{\epsilon_{si}\epsilon_0 h^2} ((11/32)Q_{inv} + Q_{dep}) \right]^{-1/3} \tag{12}$$

(12) is then included in the explicit surface potential expression given by [13]:

$$\phi_s = f + a \tag{13}$$

$$f = \phi_f + 0.5\phi_{swi} - 0.5 \left[(\phi_{swi} - 2\phi_f)^2 + 0.0016 \right]^{1/2}, \quad a = 0.025 \ln \left\{ \left[x - y (1+100y^2)^{-1/2} \right]^2 (0.16\gamma)^{-2} - 40f + 1 \right\}$$

$\phi_{swi} = \left[(V_{gs} - V_{fb} + 0.25\gamma^2)^{1/2} - 0.5\gamma \right]^2$ And ϕ_{swi} is the weak inversion surface potential, $x = V_{gs} - V_{fb} - f$, and $y = \phi_{swi} - f$. The quantum surface potential is given by

$$\varphi_{\text{sqm}} = 2\varphi_f + \delta\varphi \quad (14)$$

Using the surface potential model (13) in (9) and (10), we can calculate explicitly calculate (14). Using (14), equation (9) and 10 can be again calculate rigorously to compute quantum inversion charge density after installing. This is also shown in figure 3.

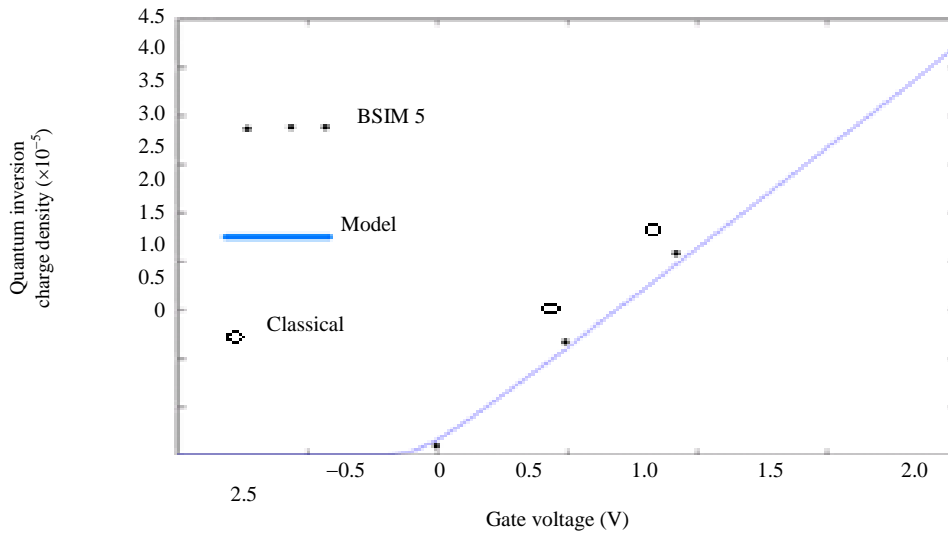


Fig. 3: Simulated results of quantum mechanical inversion charge density with gate voltage under the model parameters: substrate doping $1 \times 10^{18} \text{ cm}^{-3}$ and oxide thickness 1.5 nm. Black dots show the reported BSIM 5 results [17], round circles show the classical results and blue line show the quantum mechanical model developed.

The results in figure 2 match quite closely with the BSIM 5 results [17]. The results have been achieved by accurately modeling the shift in the surface potential. The results show that the inversion layer quantization leads to reduced inversion charge density.

4. Band gap narrowing modeling

The doping levels in sub 10nm MOSFETs are very high of the order of $1 \times 10^{20} \text{ cm}^{-3}$. The high doping levels lead to the reduction of the band-gap energy (E_g). The band gap narrowing effect is applicable to both source and the drain. The reduction in energy band-gap is given by [18].

N_D is doping concentration cm^{-3} in the source. The increase in the intrinsic carrier concentration due to excess doping is obtained by putting (15) in (16).

$$n = n_i \exp(\delta E_g / 2kT) \quad (16)$$

n_i is the intrinsic carrier concentration. The band-gap narrowing effect will reduce the built in potential existing at the source/drain and the substrate.

5. DIBL modeling

DIBL is an influence of drain potential into substrate surface potential thus lowering the potential barrier in the substrate with increasing drain-source voltage and causing increasing sub threshold currents. DIBL results in decreased concentration in the substrate due to the depletion caused by the drain potential. To account for the DIBL effect, the substrate concentration (N_b) is replaced empirically with the effective substrate concentration [19] in all the preceding equations. The substrate concentration becomes the function of the drain to source voltage and the channel length as given by (17).

$$N_B = N_b - (2\epsilon_0\epsilon_{si}V_{ds}/qL^2) \tag{17}$$

So, using (7),(14),(16) and (17) in (3), source to drain tunneling current density can be calculated as shown in figures 4,5 and 6.

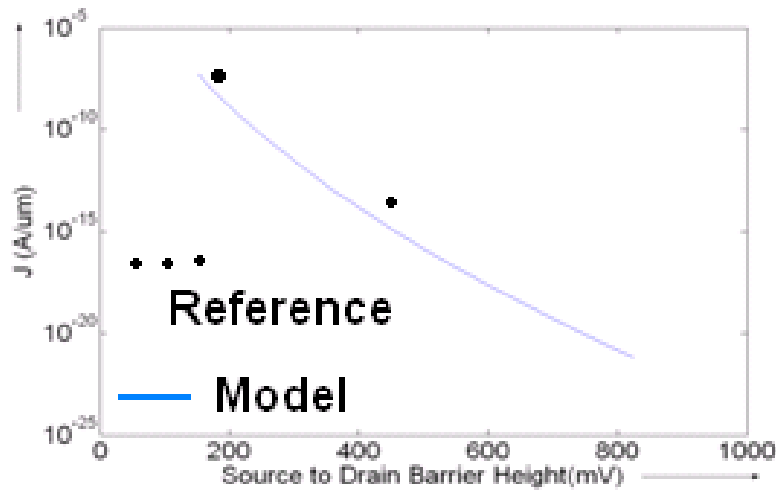


Fig 4: Tunneling current variation with the barrier height at 6nm effective channel length. Black dots show the reported numerical results [20] blue line show the model developed.

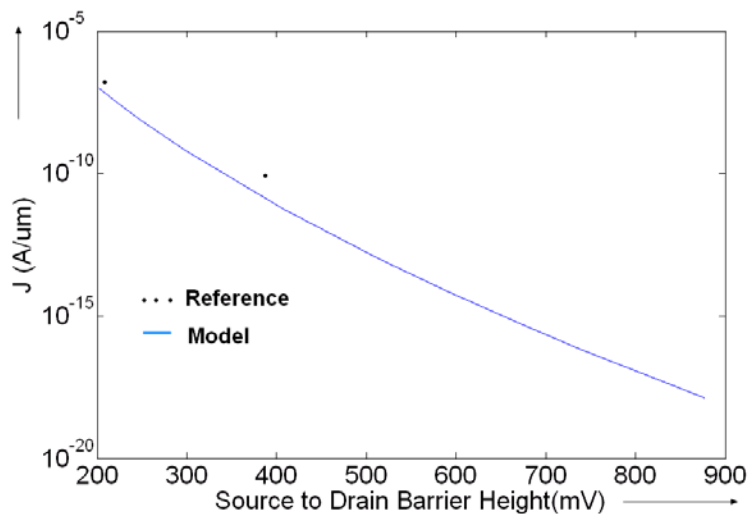


Fig 5: Tunneling current variation with the barrier height at 5nm effective channel length. Black dots show the reported numerical results [20] blue line show the model developed.

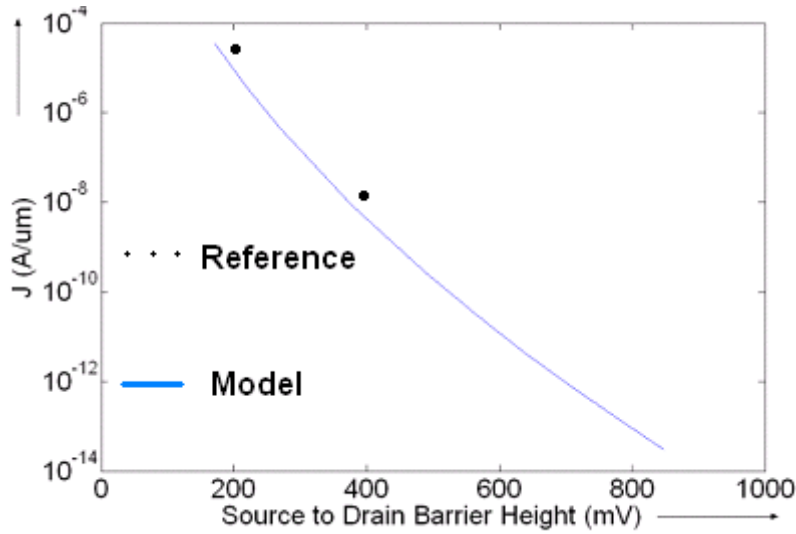


Fig 6: Tunneling current variation with the barrier height at 4nm effective channel length. Black dots show the reported numerical results [20] blue line show the model developed.

Table 1: Barrier height and source to drain quantum tunneling current variation

Barrier Height (mV) and the channel length (nm)	Tunneling Current A/um at $t_{ox}= 1.5\text{nm}$, Source doping (N_a)= $2 \times 10^{20}\text{cm}^{-3}$, Near the source doping $2 \times 10^{20}\text{cm}^{-3}$ and in the substrate $N_b=2 \times 10^{18}\text{cm}^{-3}$
400 and 4	$\sim 10^{-8}$
400 and 5	$\sim 10^{-10}$
400 and 6	$\sim 10^{-12}$

6. Results and discussion

As shown in figure 4, at effective channel length of 6nm, the quantum mechanical tunneling off currents are 10^{-6}nA/um at drain voltage of 0.5V. In figure 5, at 5nm, the quantum mechanical tunneled off currents are 0.1nA/um at a drain voltage of 0.5V. In figure 6, at 4nm, the quantum mechanical tunneled off currents are 10nA/um at a drain voltage of 0.5V. Simulation is done at source/drain doping of $2 \times 10^{20}\text{cm}^{-3}$, oxide thickness of 1.5nm and substrate doping of $2 \times 10^{18}\text{cm}^{-3}$. The results also show that at the barrier height of 200 mV, the currents increase nearly 100 times in 6nm, 5nm and 4nm geometries. The tunneling current densities increase as the barrier height is reduced. The results match quite closely with the numerical results as given in [20]. The model has been made largely analytical and it can be extended further to lower geometries for future work which was not possible accurately in [8]. The results are also summarized in Table 1.

7. Conclusion

In this paper, a rigorous and improved model has been developed for the sub-threshold direct tunneling. The increase in surface potential due to the DIBL has been modeled rigorously. Detailed modeling and physics of inversion layer quantization using variation approach has been done. DIBL modeling and its influence on substrate doping has been studied. Effect of band-gap narrowing due to high substrate doping in and near the source has been studied. Lastly, variation in substrate doping has been included in the model. The tunneling dependence with barrier height has been investigated at 6nm, 5nm and 4nm. The results indicate that the tunneling currents increase as the dimensions go down and become dominant for channel lengths sub- 4nm thus putting a limit on the scaling. The model can also be extended to the study of hole direct tunneling in p-MOSFETs operating at sub 10nm geometries and also to lower geometries. The model can also be integrated with SPICE simulators as a future work.

Acknowledgment

The authors thank the Director, UIET, Panjab University, Chandigarh, India for allowing to carry out the work. The authors would like to thank to Panjab University, Chandigarh, India for providing excellent research environment to complete this work. The authors wish to thank all individuals who have contributed directly or indirectly in completing this research work.

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