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A comparative study of quantum gates and classical logic gates implemented using Solid-State Double-Gate Nano-MOSFETs

Ooi Chek Yee[1*] , Lim Soo King[2]

[1]*Faculty of Information and Communication Technology, Universiti Tunku Abdul Rahman, Jalan Universiti, Bandar Barat, 31900 Kampar, Perak, Malaysia.*

[2]*Lee Kong Chian Faculty of Engineering and Science, Universiti Tunku Abdul Rahman, Jalan Sungai Long, Bandar Sungai Long, Cheras, 43000 Kajang, Selangor Darul Ehsan, Malaysia.*

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Abstract

The purpose of this paper is to compare the operations of silicon-based solid-state quantum computer with classical logic gate made of double-gate (DG) nano-MOSFETs. Quantum gates, such as quantum NOT gate, controlled-NOT (CNOT) and quantum register are studied. On the other hand, classical computer gates, such as NOT gate, NOR gate, NAND gate, XOR gate and XNOR gate are described. Silicon-based solid-state quantum computer operates well at extremely low cryogenic temperature (77K) as shown by oscillation of electron density profiles of the silicon-based nanodevices. Unitary matrix which specifies a valid quantum gate is proven in this study. The intrinsic delay of the classical NOT gate is calculated from simulation output data and the current-voltage (I-V) characteristic of the DG nano-MOSFET, which is used to construct the NOT gate, is plotted and studied. The motivation of this study is to investigate ways to implement quantum computer with silicon-based DG nano-MOSFET implanted with phosphorus donor atoms.

Keywords: Quantum computing; Nanodevices; Silicon semiconductor.
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1. Introduction

A quantum computer consists of two major quantum systems which have critical functions: (i) a proper quantum memory for manipulating and hosting coherent quantum superposition, this implies that electrons must behave like wave, and (ii) a quantum bus for transferring quantum information between memories [1]. Usually, quantum memories are formed by individual atoms, quantum dots or donors in solids, or even super conducting junctions. In this study, quantum memory was formed by phosphorus atom donor embedded in pure silicon lattice and this phosphorus atom becomes the qubit, which is analogous to logic bit in classical computer. Meanwhile, the quantum bus should have propagating quantum degrees of freedom such as photons (electromagnetic fields) or phonons (lattice vibrations). In this study, quantum bus is the phonons (lattice vibrations of silicon). In order to execute a quantum algorithm, the memory and the quantum bus must interact in a suitable

[*]) For Correspondence, Tel: + (60) 5 4688888 Ext: 4420, Fax: + (60) 5 4661672, E-mail: ooicy@utar.edu.my

and controlled manner. For example, if the DG nano-MOSFET which is studied in this paper is placed in strong magnetic fields at extremely low cryogenic temperatures, alignment of the phosphorus donor atom will change in parallel or antiparallel directions with respect to applied magnetic field, thereby the |0> and |1> states of the qubit will change to some superposition of the |0> and |1> states [2, 3]. This implies that electron must have wave nature instead of particle nature as in bulk MOSFETs [4]. The current challenge of quantum computer system is to upscale the quantum computer system architecture to very large sizes, but decoherence events occur at large size, as will be shown with silicon thickness variations in nano-MOSFET studied in this paper [5].

A classical computer is constructed from electrical circuit which composed of logic gates and wires while a quantum computer is built from quantum circuit consists of elementary quantum gates and wires in order to perform quantum computations. In this paper, a comparison study is carried out between some quantum gates and classical logic gates, especially NOT function [6, 7].

2. Theory

A classical bit has a state, either 0 or 1. The two possible states for a qubit are state |0> and |1>. The difference between qubits and classical bits is that besides having state |0> and |1>, a qubit can also have linear combinations of states, usually called superposition:

$$|\psi >= \alpha|0 > +\beta|1 > \tag{1}$$

Where α and β are complex numbers. Let analyze equation (1), when measure a qubit, the probability of getting result 0 is $|\alpha|^2$ whereas the probability of getting result 1 is $|\beta|^2$. From the concept of probability,

$$|\alpha|^2 + |\beta|^2 = 1 \tag{2}$$

For instance, a qubit which gives 50% $\left(\left|\frac{1}{\sqrt{2}}\right|^2\right)$ result 0 and 50% $\left(\left|\frac{1}{\sqrt{2}}\right|^2\right)$ result 1 can be written as

$$\frac{1}{\sqrt{2}}\left|0 > +\frac{1}{\sqrt{2}}\right| 1 > \tag{3}$$

The superposition state in equation (3) is denoted by |+> [3]. There are several ways to realize a qubit, (i) two different polarizations of a photon, (ii) alignment of a nuclear spin in a uniform magnetic field, (iii) 'ground' or 'excited' states, which are equivalent to |0> and |1>, of an electron orbiting a single atom. By exciting electron from state |0> to halfway between |0> and |1>, superposition state |+> is obtained, as indicated in equation (3). Method (ii) and (iii) can be used in realizing qubit in nanostructures used in this paper.

Figure 1 shown the DG nano-MOSFET structural design used in this study [8, 9, 10]. The source and drain regions of the DG nano-MOSFET are heavily n^+-doped. The donor atom used is phosphorus. For the DG nano-MOSFET in Figure 1, phosphorus donors embedded in silicon lattice is the quantum bit (qubit). The nuclear spin and electron spin

relaxation time determine the phase coherence time of the quantum computing [11]. The coherence time should be long enough in order to perform a quantum computation and read out the result.

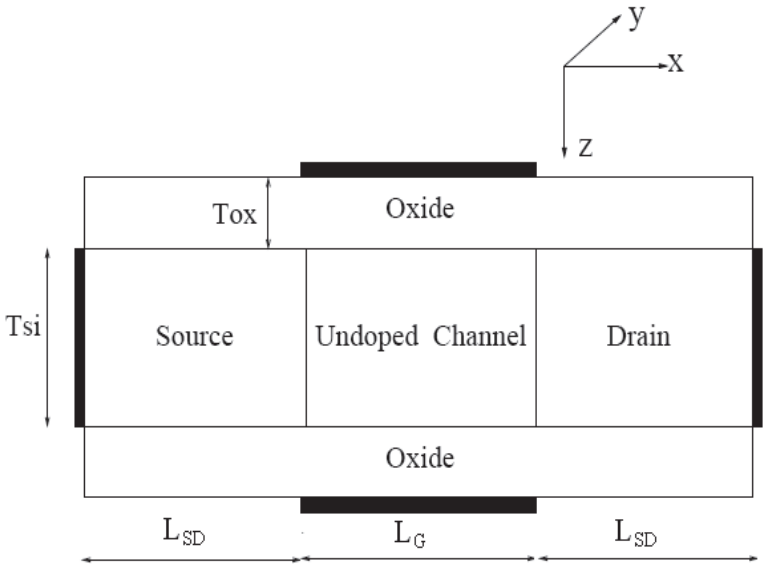

Fig. 1: 2D structural design of DG nano-MOSFET with heavily n+-doped source/drain reservoirs

In the solid-state architecture of the silicon-based nano device shown in Figure 1, the phosphorus atoms embedded in the sea of silicon lattice enable the function of quantum computations. These two elements are used for several reasons. Firstly, phosphorus is the common dopant for standard silicon-based semiconductor devices and so there are sufficient working knowledge of silicon and phosphorus in electronic industry. Secondly, these elements can meet the spin control of the quantum computer. For silicon-based quantum computer, qubit nuclear spin I=1/2 is required, and surrounding environment must be spin free, otherwise coherent states needed for quantum computation could be destroyed due to unwanted spin-spin interactions. The only stable isotope for phosphorus is phosphorus-31 which also has a spin of -1/2 nucleus. Therefore, phosphorus-31 naturally could be used to construct qubit. However, creating a spin-free silicon environment is quite difficult. Naturally, there are three isotopes for silicon: silicon-28, -29 and -30. Even-numbered silicon isotopes are spin-free whereas silicon-29 has a spin of I=1/2. Thus, in order to carry out quantum computation, silicon-29 content is greatly reduced in silicon substrate, normally in a ratio of one part in 10^5. This level of purity can be obtained with current technology [2].

The DG nano-MOSFET shown in Figure 1 has heavily n^+ doped source and drain region. The phosphorus doping concentration is $1x10^{20}$ cm^{-3}. The phosphorus lattice constant is 0.717 nm. Each source length (L_{SD}) and drain length (L_{SD}) is 7.5 nm. The channel thickness (T_{Si}) is 1.5 nm. When letting width of the nano-MOSFET in y-direction equals to 1nm, the number of phosphorus atoms in each of the source and drain volume is 1.125. So, there is one qubit at source and another one qubit at drain. When expanding the phosphorus linear array in y-direction, two separate quantum registers are formed at source and drain region. These two quantum registers convey quantum information through quantum bus formed by lattice vibrations (phonons).

Now, let compares quantum gates (particularly quantum NOT gate) with classical computer gates made up of DG nano-MOSFET (particularly classical NOT gate). The quantum NOT gate acts linearly, meaning that it transforms the state

$$\alpha|0> +\beta|1> \tag{4}$$

To the corresponding state in which the role of |0> and |1> have been interchanged,

$$\alpha|1> +\beta|0> \tag{5}$$

Quantum NOT gate can be represented in matrix form *X* as follow

$$X = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} \tag{6}$$

A quantum state $\alpha|0> +\beta|1>$ can be written in a vector notation

$$\begin{bmatrix} \alpha \\ \beta \end{bmatrix} \tag{7}$$

With top entry is the amplitude for |0> and the bottom entry is the amplitude for |1>. Then, the output for quantum NOT gate is

$$X \begin{bmatrix} \alpha \\ \beta \end{bmatrix} = \begin{bmatrix} \beta \\ \alpha \end{bmatrix} \tag{8}$$

This shows that quantum gates on a single qubit can be described by 2x2 matrixes. The matrix *X* must has the property of unitary, that is $X^{\dagger}X = I$, where $X^{\dagger}$ is the adjoint of *X* which obtained by transposing and then complex conjugating *X*. Also, *I* is the 2x2 identity matrix.

$$X^{\dagger}X = I \tag{9a}$$

This unitary constraint is the only constraint on quantum gates. Any unitary matrix specifies a valid quantum gate. Taking quantum NOT gate in equation (6) and applying equation (9a),

$$X^{\dagger}X = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} = \begin{bmatrix} 0+1 & 0+0 \\ 0+0 & 1+0 \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} = I \tag{9b}$$

The prototypical multi-qubit quantum logic gate is the controlled-NOT or CNOT gate. CNOT gate has two input qubits, which are the control qubit and the target qubit [3, 12]. Figure 2 shows this CNOT gate. In Figure 2, the top line is the control qubit and the bottom line is the target qubit. CNOT gate behaves as follow: If the control qubit is set to 0, then the target qubit is unaltered. If the control qubit is set to 1, the target qubit is inverted as expressed below.

$$|00>\rightarrow|00>;|01>\rightarrow|01>;|10>\rightarrow|11>;|11>\rightarrow|10> \tag{10}$$

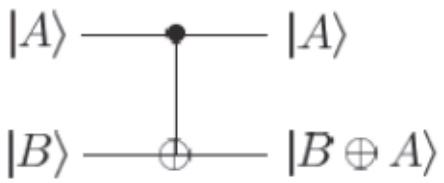

Fig. 2: The prototypical multiple qubit gate, the controlled-NOT

Another way of representing CNOT is

$$|A,B>\rightarrow|A,B\oplus A> \tag{11}$$

Where $\oplus$ is the XOR gate operation. This means that the control qubit and the target qubit are XORed together and stored in the target qubit. The matrix representation of the CNOT is as follow:

$$U_{CN}=\begin{bmatrix}1&0&0&0\\0&1&0&0\\0&0&0&1\\0&0&1&0\end{bmatrix} \tag{12}$$

In order to validate the unitary property of CNOT gate matrix, adjoint of U_{CN} which is $U_{CN}^{\dagger}$ must be obtained by transposing and then complex conjugatingU_{CN}. Finally, $U_{CN}^{\dagger}$ matrix is the same as matrixU_{CN}. Expression below proofing unitary property of CNOT gate matrix

$$U_{CN}^{\dagger}U_{CN}=\begin{bmatrix}1&0&0&0\\0&1&0&0\\0&0&0&1\\0&0&1&0\end{bmatrix}\begin{bmatrix}1&0&0&0\\0&1&0&0\\0&0&0&1\\0&0&1&0\end{bmatrix}=\begin{bmatrix}1&0&0&0\\0&1&0&0\\0&0&1&0\\0&0&0&1\end{bmatrix}=I \tag{13}$$

Logic gates in classical computer are formed by transistors. In this paper, DG nano-MOSFETs with channel length 10 nm are used as the components to build those logic gates in classical computer. The transistor levels of basic logic gates are presented with emphasis on NOT gate. NOT gate is formed by loaded nano-MOSFET. When the input of this NOT gate is 0, the output is 1. On the other hand, when the input to the same NOT gate is 1, the output is 0. The intrinsic delay τ of this NOT gate is given by the following expression

$$\tau=\frac{\Delta Q}{I_{eff}} \tag{14}$$

Where ΔQ is the charge difference between the two logic states and I_{eff} is the effective drain current [13]. For technology scaling factor of s, delay τ is scaled down by s to τ′ as shown below

$$\tau' = s\tau \tag{15}$$

So, nano-MOSFET loaded NOT gate has faster switching speed than logic NOT gate formed by bulk MOSFETs [14, 15, 16].

3. Results and Discussion

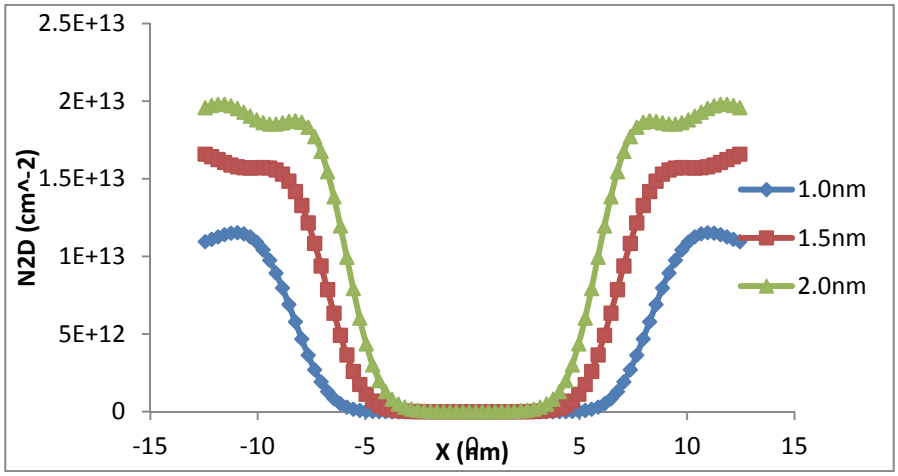

Fig. 3: Normal plot of 2D electron density along the channel for various silicon channel thicknesses at 77K using quantum model

Figure 3 shows the 2D electron density profile along the channel of DG nano MOSFET for silicon channel thickness values of 1.0 nm, 1.5 nm and 2.0 nm. The simulation temperature was 77 K and the quantum model electron transport was used in the simulation using nanoMOS simulation tool [17, 18, 19]. The nano-MOSFET was simulated at equilibrium condition with all biasing voltages set to zero volt. At source and drain region, electron density profiles show oscillation interference behavior because electron behaves like wave at cryogenic low temperature (77 K) for nanodevices. This phenomenon is important to build quantum computer. The source and drain were doped with phosphorus donor atoms which are the qubits for quantum computation. The qubits at source and drain convey quantum information through quantum bus form by lattice vibrations through the channel. When analyzing this oscillation behavior, the following relationships are used

$$\mathrm{f} = \frac{\mathrm{v}}{\lambda} \tag{16}$$

$$\mathrm{T} = \frac{1}{\mathrm{f}} \tag{17}$$

Where f=frequency, v=velocity, λ=wavelength, T=period. At T_{Si}=1.0nm, λ=4x6nm=24nm, average electron velocity at 77K was around $2x10^{-2}$ m/s. Equation (16) gives f=$833x10^{3}$Hz, equation (17) gives T=1200 ns (nanosecond) which was the coherence time. At T_{Si}=2.0nm, λ=9nm, average electron velocity at 77K was around $2x10^{-2}$ m/s. Equation (16) gives f=$2.2x10^{6}$Hz, equation (17) gives T=450 ns (nanosecond) which was the coherence time. So, as T_{Si} increases, coherence time reduces. T_{Si}=1.0nm has larger λ than T_{Si}=2.0nm. Smaller T_{Si}=2.0nm has smaller λ and thus show more oscillation cycles. T_{Si}=1.0nm exhibits lesser oscillation cycles due to larger λ. From the coherence time analysis, larger T_{Si} has smaller coherence time. This causes a major problem in scaling up the number of qubits in quantum computers. This problem is seen , for example, when using Peter Shor's algorithm for finding the prime factors of numbers used in public-encryption systems (numbers which usually consist of more than a hundred digits) [2]. Since this task requires a quantum computer with several thousand qubits, solid-state quantum computers are a good candidate for scaling up the quantum computer. The current challenge in any quantum computer architecture is to scale the system to very large sizes but larger sizes tend to have computation errors cause by decoherence. This sizing issue has to be solve first when want to implement large scale quantum computers.

In order to let the qubit at source and drain to perform quantum logic gate functions, the DG nano-MOSFET structure must be simulated at cryogenic low temperature (77 K) because at room temperature 300 K, the wave nature of electron disappear and electron behaves like particle already. The simulated drain current versus gate voltage (I-V) graph for DG nano-MOSFET at 77 K non-equilibrium condition is shown in Figure 4 [20, 21].

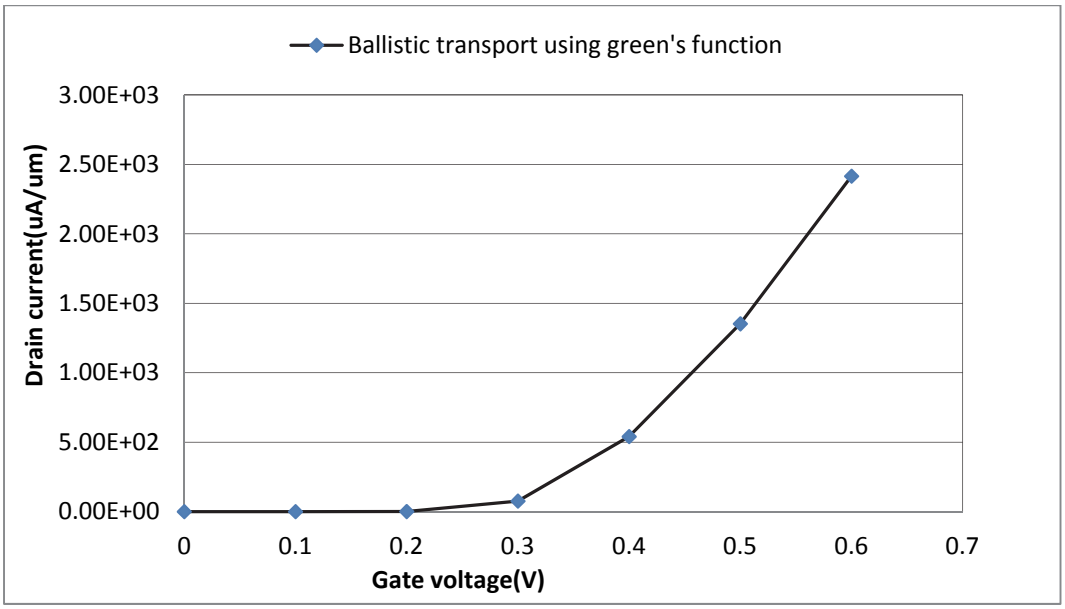

Fig. 4: Normal plot of drain current vs gate voltage sweep at 77 K using quantum model transport model

The electron transport model used in the simulation of Figure 4 is the ballistic transport using Green's function [14, 15, 16]. Next, let analyze the classical NOT gate constructed from DG nano-MOSFETs. Figure 5 shows the transistor level schematic diagram. The intrinsic delay of this NOT gate is given by equation (14), the electron density for on-state and off-state of DG nano-MOSFET were $2x10^{12}$ cm^{-2} and $1x10^{8}$ cm^{-2}, respectively. The on-state drain current from Figure 4 is 2500 μA/μm. The channel length is

10 nm and electronic charge is e=1.602x10^{-19} C. So, by using equation (14), intrinsic delay time for this classical NOT gate is 12.8 fs. This NOT gate should be faster in switching time than NOT gate constructed with bulk MOSFET. The transistor level schematic diagrams for other basic classical logic gates used in classical computer are presented below.

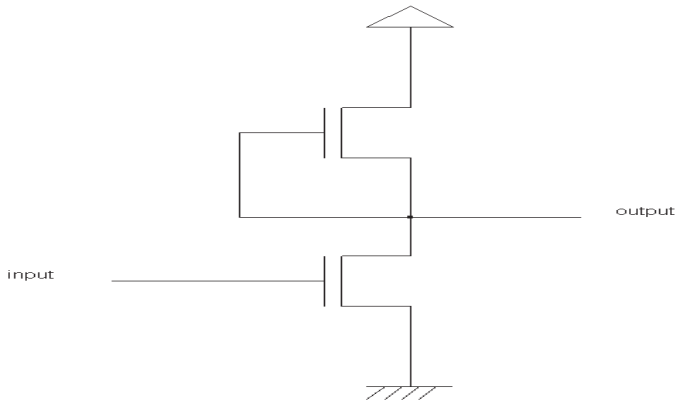

Fig. 5: Transistor level schematic diagram of classical NOT logic gate constructed from DG nano-MOSFETs

Figure 6 shows the loaded MOSFET NOR gate. Figure 7 shows loaded MOSFET NAND gate. Figure 8 shows loaded MOSFET XNOR/XOR gate. The quantum gates version of these classical logic gates can be implemented using CNOT gates (controlled-NOT) of multiple qubits.

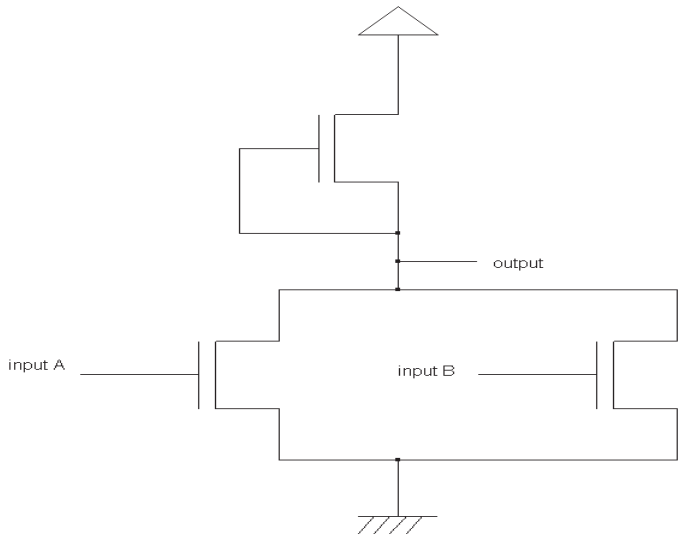

Fig. 6: Transistor level schematic diagram of classical NOR logic gate constructed from DG nano-MOSFETs

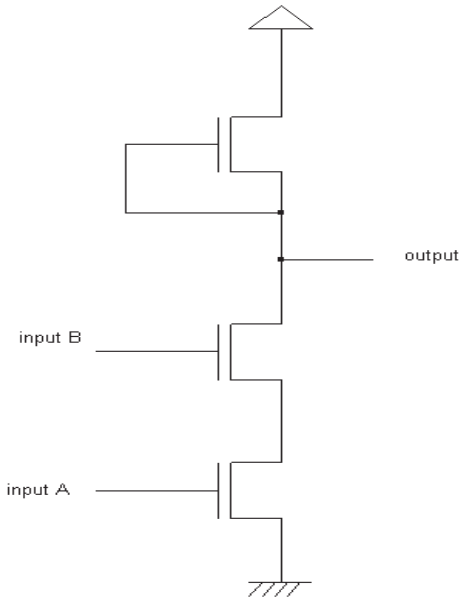

Fig. 7: Transistor level schematic diagram of classical NAND logic gate constructed from DG nano-MOSFETs

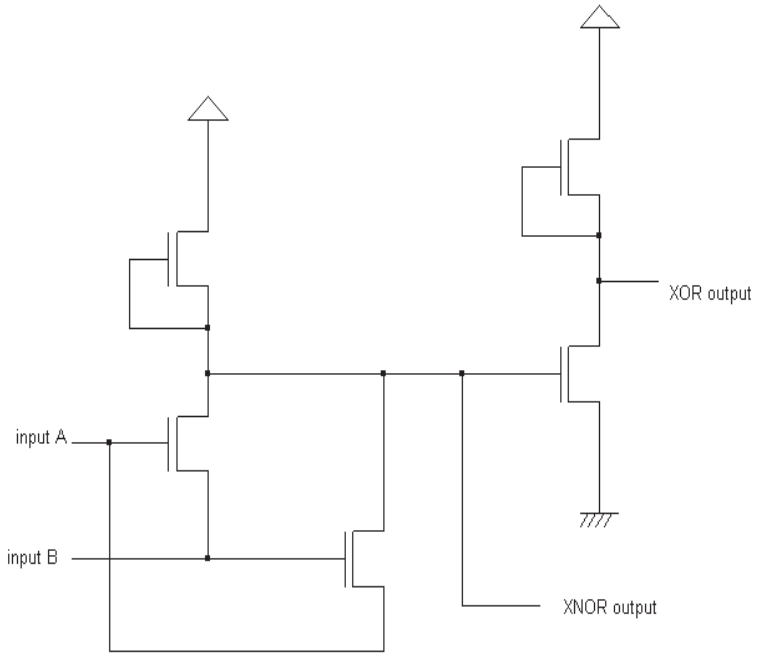

Fig. 8: Transistor level schematic diagram of classical XNOR/XOR logic gate constructed from DG nano-MOSFETs

4. Conclusion

One of the challenges faced in quantum computing is to scale up the number of qubits for quantum computation. Silicon-based solid-state quantum computer is a good candidate since current silicon semiconductor technology knowledge is very mature. Silicon-based nanodevice is suitable for creating qubits by using phosphorus atoms. The qubits are able to perform basic quantum gates which are needed when implementing quantum computer. These quantum computations should be carried out at cryogenic low temperature (77 K) where electron behaves like wave. On the other hand, classical computer logic gates can also be implemented by using silicon nanodevices. In these classical logic gates, silicon nanodevices are used to create the transistor levels of the logic gates. A qubit (or QUantum BIT) can hold not only the states |0> and |1> but also a linear superposition of both states. A classical logic bit has only two logic states, which are 0 and 1.

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