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# Two dimensional simulation and analysis of density-of-states (DOS) in top-gated nanocrystalline silicon thin film transistor (nc-Si TFT)

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**Abstract**

In this paper, we have presented the effect of the density-of-states (DOS) parameters on the performance of n-channel top gated staggered nc-Si TFT. The analysis was performed using ATLAS 2D TCAD simulator from SILVACO. The variation in DOS in nc-Si material and thus on the TFT device performance occurred by altering the channel length and channel quality is presented. The simulation results reveal that the increase in channel length and the degradation in channel quality degrade the trans-conductance and drain current. By iterating the order of parasitic resistance and the value of characteristic decay energy related to material quality, the same trend is achieved for simulated and experimental results for nc-Si TFT with W/L=200μm/50μm.

**Keywords**: Nanocrystalline silicon; Thin film transistor; TCAD; ATLAS; Channel length; Density of states.

## 1. Introduction

The nanocrystalline silicon (nc-Si) has several advantageous features including enhanced mobility [1] and better stability [2, 3] over amorphous silicon (a-Si) and it also provide structural uniformity and low fabrication cost [4] when compared with polycrystalline silicon (poly-Si) [5-11]. Therefore nc-Si has received huge attention to be used as thin film transistor (TFT) channel layer in various display applications like active matrix organic light emitting diode (AMOLED) [12], medical X-ray imagers [13] and radio frequency identification devices (RFID) tags [14]. Based on the level of the gate electrode, the TFTs are divided into two types; top gated TFT and bottom gated or inverted TFT. In top gate TFT, the gate electrode is located above the semiconductor layer, whereas in bottom gate TFT, the gate electrode is located below the semiconductor layer.

Limited papers have been published based on the numerical simulation of nc-Si TFT [15-17] Dosev et. al. [15] provided the numerical simulation results for inverted staggered TFTs using SiO2 dielectric and presented the influence of acceptor-like defect states density on transconductance. They examined that the acceptor-like defect states in nc-Si:H are filled at much lower gate voltages than in a-Si:H TFTs having similar threshold voltages. The transconductance shape of nc-Si:H TFTs has a shape typical for a-Si:H TFTs before the

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acceptor-like states are filled. When electrons fill the acceptor-like states, the transconductance of nc-Si:H TFTs become typical for poly-Si TFTs. The reason for this behavior is the density of acceptor-like states, which situates the nc-Si:H TFTs properties between a-Si:H and the poly-Si transistors. However, authors [15] considered an optical gap of 1.91 eV which is not a normal value neither for a-Si:H nor for nc-Si:H devices. For devices with a gap of 1.72 eV, M. Estrada et. al. [16] demonstrated that the anomalous effect of the transconductance is related to the trapped charge concentration characteristics and observed that the acceptor tail states activation energy is similar to the normal values for a-Si devices of 0.035eV, provided that some conditions are met regarded the concentration of trapped charges in tail and deep states and the free charge concentration in the material, which doesn't necessarily suggest a behavior in between a-Si:H and poly-Si. Archontas et.al. [17] proposed the electrical behavior of inverted staggered TFTs using Si3N4 as gate dielectric and presented the transfer and output characteristic of inverted staggered nc-Si TFTs with different channel lengths. They have found that in the off-state region, the conduction mechanism at less negative gate voltages was attributed to thermal generation while in case of high negative gate voltages (<-15 V), the leakage current was due to the band to band tunneling mechanism.

When the nc-Si:H film is deposited over the amorphous substrate like glass, then its crystallinity is not very high in the initial growth phases because the nc-Si:H is usually grown up in the form of cone-shape that is from bottom to top. The crystallinity increases with the increase in nc-Si:H film thickness [18] This structural difference in top and bottom layers of nc-Si:H film plays crucial role in designing nc-Si:H TFT. In the case of bottom-gate structure, the device performance depends on the bottom layer of nc-Si:H film where the channel is formed as compared to top-gate TFT, where the channel is located in highly crystalline part at the top of nc-Si:H film [19]. Owing to this, the top-gate nc-Si:H TFT provides high field effect mobility (μFET) i.e. in range of 40 cm2/Vs [20] to 150 cm2/Vs [7] as compared to bottom-gate TFT which have μFET as 0.5-3 cm2/Vs [21, 22] Therefore, in this paper we have presented the numerical simulation of top-gate staggered nc-Si TFT at various channel lengths and characteristics of decay energy which has not been explored by other research groups [15-17] .

In the present work, for the device simulation of top-gate nc-Si TFT, the high-k gate dielectric i.e. Si3N4 is considered in place of SiO2 because Si3N4 shows high capacitance densities with wider tunneling barrier, high breakdown field and less interface trap density as compared to SiO2 and hence provide better electrical stability in nc-Si TFT [23].

## 2. Theory and Model

Hot wire chemical vapour deposition (HWCVD) method is commonly used for the deposition of nc-Si:H over glass substrate. The resulting nc-Si:H film consists of small silicon crystallites than poly-Si, with an average grain size of a few nanometers, embedded into a-Si:H. It provides the possibility of direct deposition of nc-Si:H at a very low temperature over a large area and at high deposition rates [24]. However, the low temperature process used for nc-Si deposition as well as the amorphous nature of non-crystalline substrate (like glass) lead to the formation of material having missing atoms. Deep defect states in the forbidden energy gap of the nc-Si are associated with these missing atoms, i.e. dangling bonds [25]. Deep defect states are also associated with the deviation in bond length and angle which results in states below the conduction band, known as band tail states [26]. DOS in nc-Si (as depicted in Figure 1) is composed of two Gaussian distributed deep defect states (acceptor-like and donor-like deep states) and two exponentially distributed band tail states (acceptor-like and donor-like tail states). The density of states

that are presented in the upper half region of the band gap acts as the acceptor like states whereas the states that are in the bottom half region of the band gap acts as the donor-like states. The acceptor-like states are negatively charged when they are occupied and neutral when they are unoccupied. However, the donor-like states are positively charged when they are unoccupied and neutral when they are occupied [27].

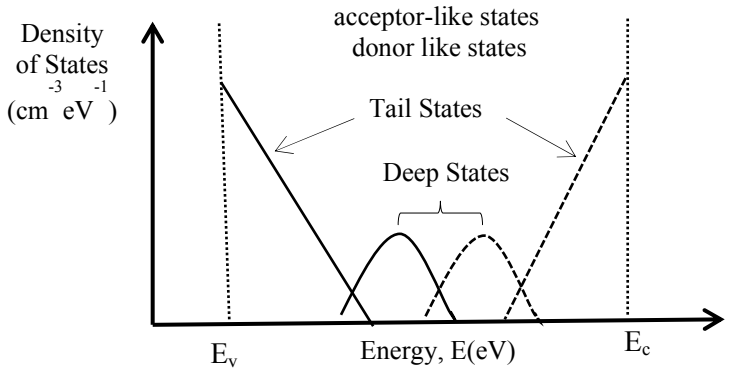


Figure 1: Density of states within the band gap of nc-Si

DOS in nc-Si TFT is highly influenced by the parasitic resistance associated with the geometrical aspects like channel length [28,29,17] and also by the quality of channel layer [15]. Parasitic resistance component, R in n-channel top gated staggered TFT as shown in Figure 2 consists of series resistance of active layer (Rch) and insulating layer (Ri), series resistance of contact layers (Rs) and contact resistance (Rc) between metal electrode and source/drain contacts, given by:

$$R = R_{ch} + R_i + R_s + R_c \quad (1)$$

Therefore, parasitic resistance can strongly influence the transconductance and drain current of the TFT device. Therefore, deepe investigation of parasitic resistance is required for the further enhancement of TFT performance.

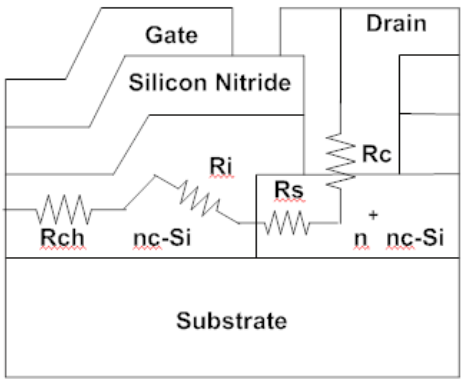


Figure 2(a)

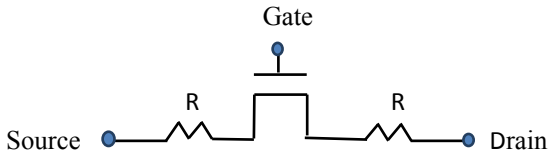


Figure 2(b)

Figure 2: (a) Parasitic resistance (R) components of the n-channel top gated nc-Si TFT and (b) Equivalent circuit of the TFTs used for device simulation

DOS model, which is available in TFT module in ATLAS tool package, is used to extract the density of states present in the band gap of nc-Si. We have considered the case that DOS has a continuous distribution from the band tail states to the extended energy states. DOS can be defined as a function of energy as follows:

$$g(E) = g_{GA}(E) + g_{GD}(E) + g_{TA}(E) + g_{TD}(E) \quad (2)$$

Where

$$g_{GA}(E) = NGA \ \exp\left[-\left(\frac{EGA - E}{WGA}\right)^2\right] \quad (3)$$

$$g_{GD}(E) = NGD \ \exp\left[-\left(\frac{E-EGD}{WGD}\right)^2\right] \quad (4)$$

$$g_{TA}(E) = NTA \ \exp\left(\frac{E-E_C}{WTA}\right) \quad (5)$$

$$g_{TD}(E) = NTD \ \exp\left(\frac{E_V-E}{WTD}\right) \quad (6)$$

where $E_C$ and $E_v$ are the conduction and valence band edge energies, $E$ is the trap energy, $N$ is the edge intercept density, $W$ is the characteristic decay energy and the subscripts ($T$, $G$, $A$, $D$) stand for band tail, Gaussian deep, acceptor and donor states respectively.

## 3. Simulation and Analysis

Figure 3 shows the virtually fabricated TFT structure used for 2D device simulation on ATLAS by SILVACO. Table 1 shows the value of various nc-Si TFT parameters used for device simulation.

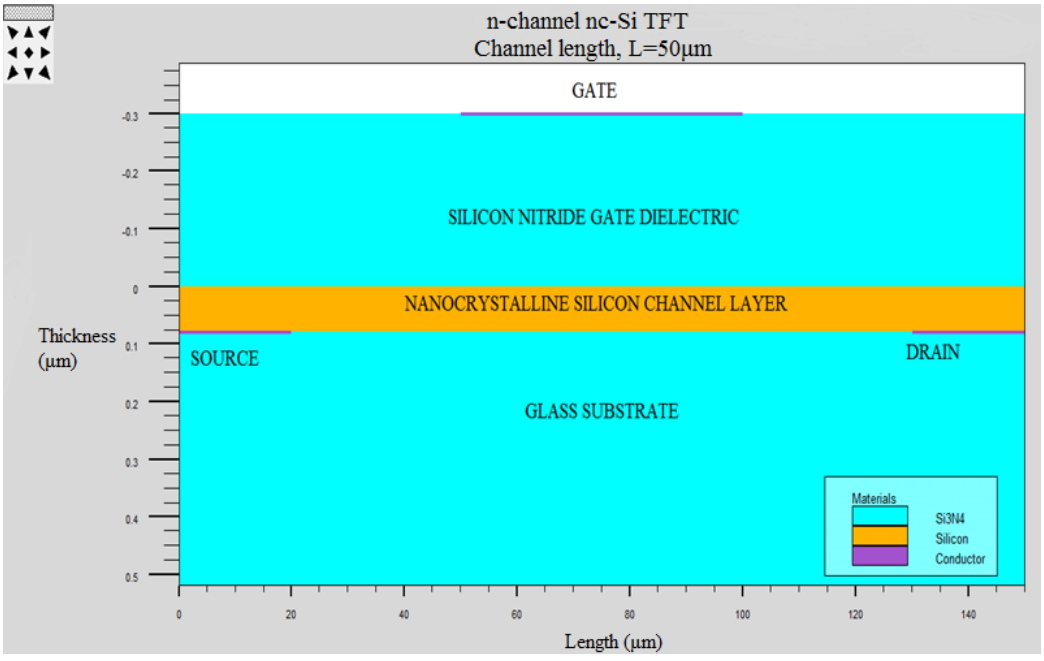


Figure 3: nc-Si TFT structure for ATLAS simulation

The nc-Si is used as an active layer with a thickness of 80 nm and the 300 nm thick $Si_3N_4$ layer is used as a gate dielectric. The width of the device is taken as 200µm and the device length range varies from 50µm to 90µm. The drain voltage, $V_{DS}$ is fixed at 10V. In spite of defining a new layer, the source and drain regions are implemented using highly

doped (i.e. $10^{20}$ /cm$^3$) n+ region and the aluminum metal contact on the top of it. The parasitic resistance is employed as a lumped component in the simulation input desk separately and is not defined in the mesh structure.

The influence of DOS (i.e. the nc-Si material properties) on the nc-Si TFT performance is investigated by considering different values of characteristic decay energy (WTA) as 0.020, 0.025, 0.033, 0.030, 0.040 eV and keeping parasitic resistance value fixed at $10^6$ Ω. The higher value of WTA relates to the wider acceptor like tail states, which corresponds to the film, which has more amorphous-like properties and thus higher parasitic resistance. Similarly, the lower value of WTA defines that the film is more polycrystalline.

The simulation results reveal that the transconductance degradation (as shown in Figure 4) occurs as the film become more amorphous or as the value of WTA increases from 0.020 to 0.040eV. This transconductance degradation due to the variation in material quality causes the reduction of drain current as illustrated in Figure 5 and thus limits the on-current of a device.

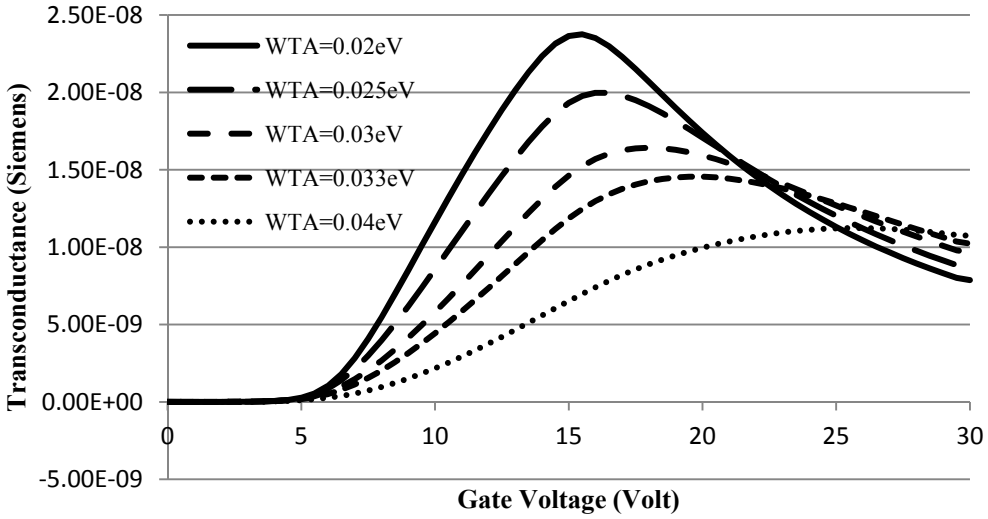


Figure 4: Variation of transconductance as a function of gate voltage for different values of tail states

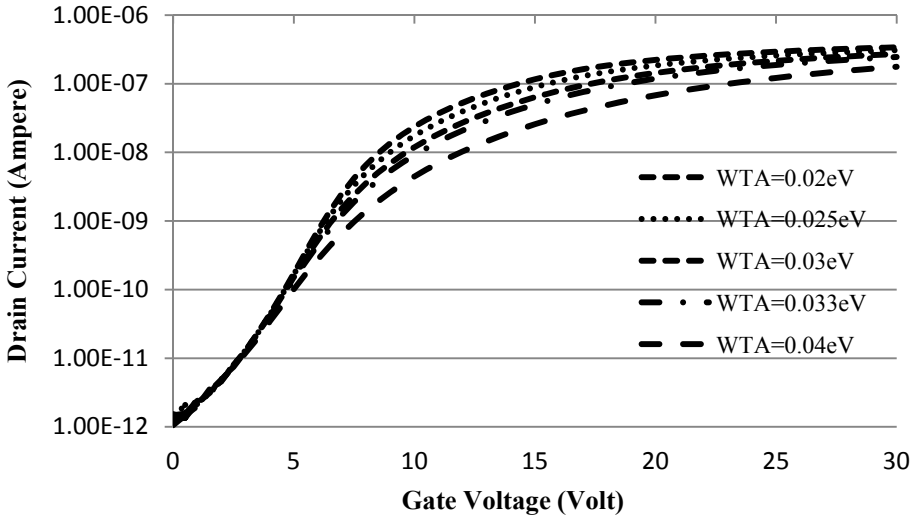


Figure 5: Variation of drain current as a function of gate voltage for different values of tail states

The channel length dependence on the drain current of nc-Si TFT is analyzed by varying the channel length from 50 to 100μm while maintaining other parameter like DOS as fixed at initial fitting values (i.e. WTA=0.02eV). The simulation results indicate that an increase in channel length degrades the transconductance as shown in Figure 6 and hence the drain current as shown in Figure 7. This drain current degradation is attributed due to the increase in overall parasitic resistance due to the increase in weight of the series resistance of the channel layer. The drain current degradation can also be explained by the increase of the transverse electric field on increasing the channel length even if the channel depth remains fixed. This variation is illustrated in Figure 8 for the channel length values of 50μm and 90μm.

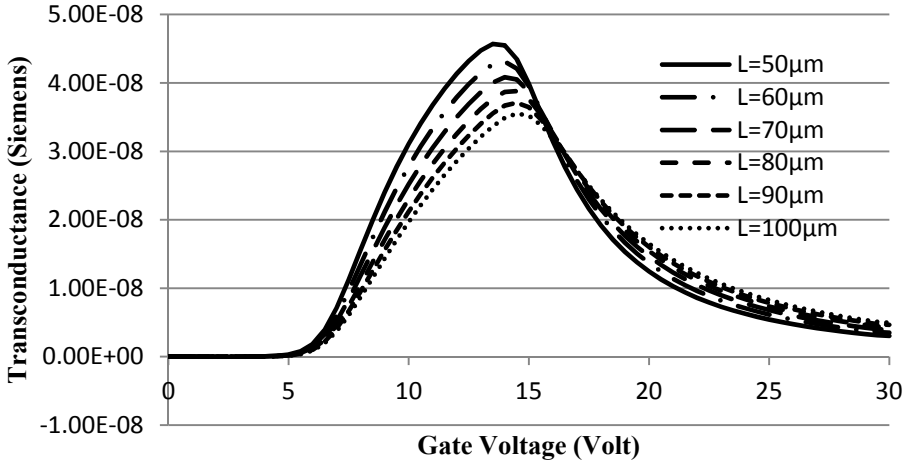


Figure 6: Variation of transconductance as a function of gate voltage for different values of channel length

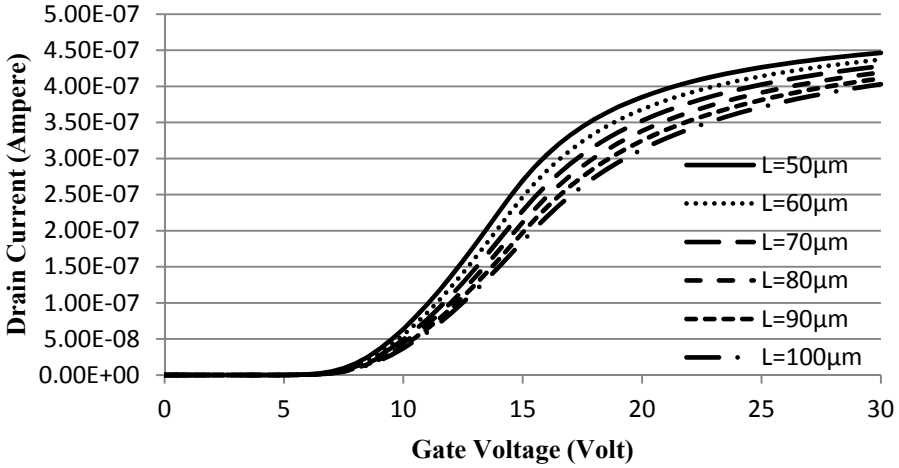


Figure 7: Variation of drain current as a function of gate voltage for different values of channel length

The dependence of parasitic resistance on the transconductance is analyzed by varying the parasitic resistance, R from $10^3$ to $10^7$ Ω and considering the fixed value of WTA as 0.02eV. The simulation result shown in Figure 9 reveals that the transconductance decreases as the parasitic resistance increases from $10^3$ to $10^7$ Ω. This increase in R value is

due to the increase in the series resistance of the channel layer with the increase in channel length.

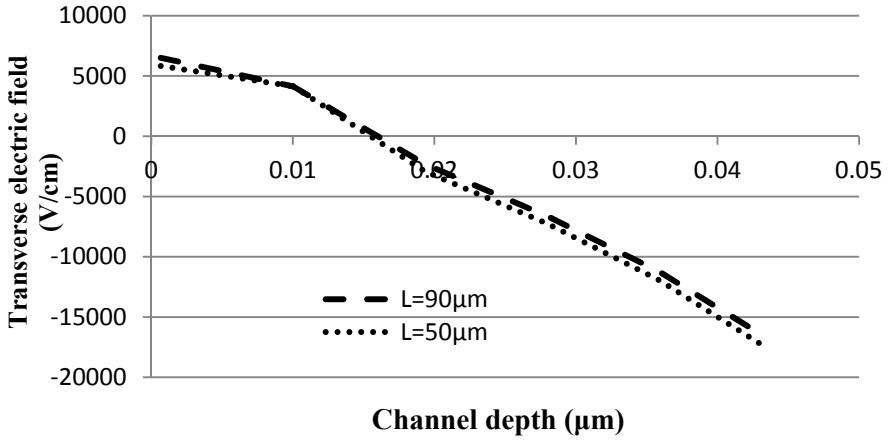


Figure 8: Channel length dependence on Transverse electric field

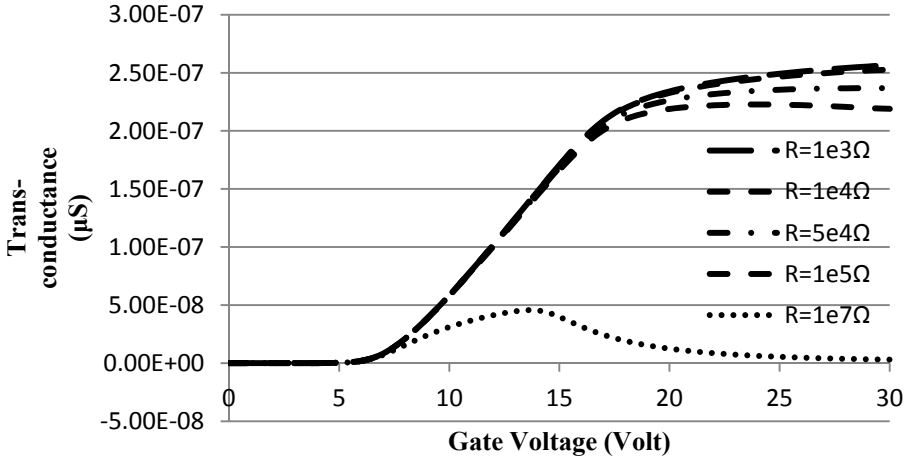


Figure 9: Variation of transconductance as a function of gate voltage for different values of parasitic resistance

Table 1: ATLAS device simulation parameter for nc-Si TFT

| Parameter | Description | nc-Si | |
|---|---|---|---|
| NTA | Conduction band edge intercept tail states density | $1x10^{20}$ | $cm^{-3}$ |
| NTD | Valence band edge intercept tail states density | $1x10^{20}$ | $cm^{-3}$ |
| NGA | Conduction band edge intercept deep states density | $3.7x10^{17}$ | $cm^{-3}$ |
| NGD | Valence band edge intercept deep states density | $3.7x10^{17}$ | $cm^{-3}$ |
| EGA | Peak energy of deep states as $E=E_C$ | 0.4 | eV |
| EGD | Peak energy of deep states as $E=E_V$ | 0.4 | eV |
| WTA | Characteristic decay energy of tail states as $E=E_C$ | 0.025 | eV |
| WTD | Characteristic decay energy of tail states as $E=E_v$ | 0.025 | eV |
| WGA | Characteristic decay energy of deep states as $E=E_C$ | 0.1 | eV |
| WGD | Characteristic decay energy of deep states as $E=E_v$ | 0.1 | eV |

Figure 10 shows the comparison between simulated and experimental results of Lee at. al. [30]. In simulation, the value for WTA and R is kept fixed at 0.02eV and $10^6$ Ω, respectively. In order to compare the simulated results with the experimental findings, a modeling factor N=exp(α) is used where the value of α is taken as 0.27. This factor will compensate the difference between the simulated DOS value and actual DOS in nc-Si film used in device fabrication. The simulated drain current results show similar trends with experimental variation. However, the deviation from the experimental results is attributed due to the fact that the experimentally fabricated device may have different DOS value due to different nc-Si material quality.

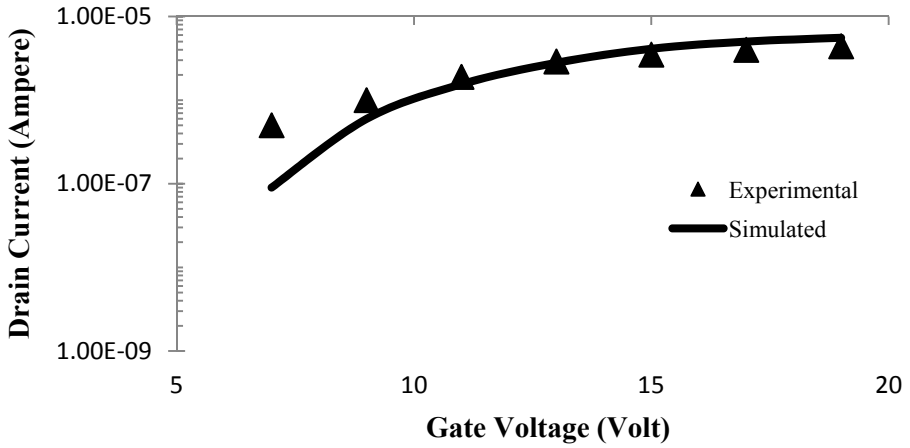


Figure 10: Plot of the transfer characteristic of nc-Si top-gated TFT (W=200μm and L=50μm) simulated at $V_{DS}$=10V for WTA=0.02 and R=$10^6$ Ω. Solid line shows the experimental results of C.H.Lee et. al. [30] and dotted line shows simulated results

## 4. Conclusion

The effects of DOS and channel length on the performance of nc-Si TFT has been investigated using ATLAS 2D device simulator by SILVACO. The simulation results reveal that the channel material properties affect the device transconductance due to the increase in the value of characteristic decay energy. This causes the increase in DOS and therefore degrades the drain current which in turn limits the on-state device performance. It has been also observed that the increase in channel length also degrades the transconductance and drain current due to increase in weight of parasitic resistance. The outcome of this study is compared with the experimental data and the similar trend between the two has been observed.

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