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Dielectric Effects on Graphene Field Effect Transistors Studied with an Iterative Simulation Approach

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ABSTRACT

A simulation method has been formulated to study the characteristics of a Graphene Field Effect Transistor (GFET). The method takes care of the effect of source and drain contact resistances while iteratively solving for the drain current. The results when compared with experimental data validate our modeling and simulation approach. The method has been used to investigate the effect of different gate dielectric materials and their dimensions on the output as well as transfer characteristics of the GFET. Our results open new ways for the possibility of dielectric engineered GFET characteristics suiting to the requirement of a given device application. The convergence of the point of inflexion for dual positive gated GFETs is interesting. The existence of a critical thickness for each dielectric material, beyond which the current saturates and the rise in its value with dielectric constant(ε_r), are some novel features worth attention.

Keywords: Dielectric, FET, Graphene, Simulation.

1. INTRODUCTION

A single layer of graphite has changed the entire scenario of the electronics industry due to its two-dimensional (2D) structure and Dirac fermion behaviour of electrons and holes. This revolutionary 2D material named Graphene was first isolated at the University of Manchester in 2004 [1, 2]. Graphene exhibits a wide range of exotic properties, such as Veselago lensing [3], Klein tunnelling [4-7], edge state mixing [8-11], and the wedding cake structure of quantum hall states [12]. It has attracted enormous interest of the electron device community due to its exclusive properties, relevant for the electronic applications [11, 12]. The intrinsically high mobility makes graphene a promising material for ultra-fast electronics operating in the THz frequencies [13]. Due to the unusual band structure of graphene, the sheet carrier density is tuned continuously between electrons and holes and this unique arrangement of graphene allows the electrons to move easily with extremely high velocity without the significant chance of scattering resulting in saving the energy, typically lost in other conductors. The carrier transport in graphene is similar to that of massless particles [14] and it conducts heat in all directions, works as an isotropic conductor. These exceptional properties of graphene play a vital role to make it suitable for a future high-speed field effect transistor. According to the International Technology Roadmap for Semiconductors, the strategic planning document for semiconductor industry, graphene is among the candidate materials for the silicon substitution. Graphene Field Effect Transistor (GFET), the most straightforward device application of graphene, may seem to be a replacement channel material for silicon Metal Oxide Semiconductor Field Effect Transistors

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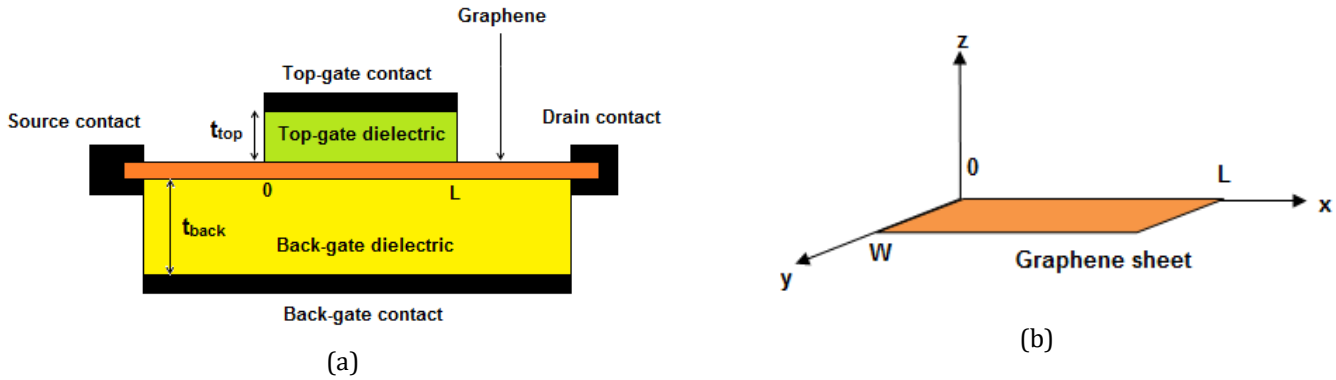
(MOSFETs) and today a growing number of groups are successfully fabricating graphene transistors. The most specific benefit of GFET is the scaling up of the drain current by increasing the device channel width, bearing a great significance for realizing high-frequency graphene devices with sufficient drain current for large circuits and associated measurements. Furthermore, it has been shown that graphene devices exhibit current amplification in the microwave frequency range [15]. The intrinsic current gain of the graphene transistors was found to decrease with increasing frequency and follows the ideal $1/f$ dependence expected for conventional FETs. These beneficial features suggest a conventional FET-like behaviour for graphene transistors. Though these GFETs are based on the common principle of conventional MOSFET, they suffer from some difficulties. The absence of required bandgap makes it difficult to achieve very high on/off switching ratio resulting in the transistor incapable to turn-off. In order to overcome these difficulties, researchers are motivated to explore new graphene device concepts, such as the tunnel FETs [16-19], the bilayer pseudospin FETs [20], the Graphene Base hot-electron Transistors (GBT) [21] and the SymFET [22].

The most often studied graphene FET structure is a back-gated configuration. The top- and dual-gated graphene are more suitable for commercial applications whereas, the back and side gates in graphene FETs are considered as optional features. Top gating graphene FET helps to control the carrier concentration in the graphene channel. This is because top gating offers an additional degree of freedom in changing the dielectric material as well as the thickness. As we have noted, the electronic properties of GFET are seriously affected by the gate dielectric [23]. The choice of the gate dielectric material and deposition technique are two most important factors for the behaviour of graphene-based FETs. The deposition of dielectrics is usually a problematic issue because of trapping of charges which affects the carrier mobility and also shifts the transistor threshold voltage.

The low ε_r of SiO_2 is the main impediment of Si technology for CMOS scaling issues. That is why researchers have dwelt upon seeking dielectric materials with higher ε_r [24]. The device and material communities have experimented with many of the dielectric materials for compatibility with graphene [25-28]. In an attempt to address this issue, we have first developed a simulation method for GFET which has an excellent agreement with experimental data. The method is then used to study the effects of various dielectric materials and their dimension on the characteristics of GFETs. It is interesting to note from our results that there is a testimonial convergence of all the inflection points in the output characteristics of the GFETs with different ε_r when the back-gate voltage is positive. Further, it is very interesting to note that the drain current saturates after a critical thickness and that such thickness increases with ε_r.

2. DESIGN CONSIDERATION

The GFETs are normally of four different typical configurations. These are the so called back-gated [29], top-gated [30], dual-gated [31] and the side-gated GFETs [32]. These four different structures of graphene have been already demonstrated on exfoliated [33], epitaxial [34] and CVD-grown graphene [35]. In our simulation study, we have used the dual gating configuration of GFET and its schematic diagram is presented in Figure 1(a). It has four terminals namely source, drain, back-gate and top-gate. Different dielectric layers have been considered in this work for separation of the two gate electrodes from the channel (Table 1).



(a) (b)

Figure 1. (a) Schematic diagram of the Graphene Field Effect Transistor (GFET), (b) coordinate system used for the graphene channel analysis.

The coordinate system used for the formulation has been shown in Figure 1(b). Due to 2D effect, carriers are confined in the z-direction and hence their motion is restricted to the x-y plane. Further, we assume uniform transport properties for the graphene in the y-direction and hence the formulation basically reduces to a one-dimensional transport. We have considered six GFET structures for the present study. Six different dielectric materials compatible with graphene have been selected as the top-gate dielectric layer while the back-gate dielectric is assumed to be SiO_2 for all the GFETs. The ε_r of those six top-gate dielectric materials and their corresponding GFET structure names are presented in Table 1.

Table 1 Top-gate dielectrics and corresponding GFET structure

Dielectric Name	Dielectric Constant (ε_r)	GFET Structure Name
Fluorinated Graphene (FG)	1.2	G1
Silicon Nitride (Si_3N_4)	7.5	G2
Aluminium Oxide (Al_2O_3)	9.0	G3
Yttrium Oxide (Y_2O_3)	10.0	G4
Hafnium Oxide (HfO_2)	16.0	G5
Zirconium Oxide (ZrO_2)	23.0	G6

The above mentioned GFET structures are used to simulate the GFET characteristics for different values of top-gate dielectric layer thickness varying from 10 nm to 400 nm.

3. MODELING AND SIMULATION

In GFET the objective of a basic modelling approach is to derive an expression for the drain current. In general, the drain current I_{DS}, of a typical GFET (Figure 1) passing through any cross section of the channel at position x, can be expressed as:

where q is the elementary charge, ρ_s (x) and $v(x)$ are respectively the free carrier sheet density

$$I_{DS} = -q\rho_s(x)\, v(x)W \tag{1}$$

and electron velocity in the channel at position x, and W is the channel width transverse to the direction of current flow. The sheet charge density, in the graphene channel, can be attributed to four different sources such as (i) the intrinsic charge, (ii) the charge due to quantum capacitance, (iii) the charge induced by the gate bias and (iv) the charge due to intentional or un-intentional doping.

In an undoped graphene layer in thermal equilibrium, there are moving electrons in conduction band (CB) and holes in valence band (VB), which are similar to intrinsic carriers in a pure semiconductor. To determine the intrinsic charge density, we start with the dispersion of mobile electrons in graphene in the first Brillouin Zone (BZ) given by

$$E(k) = s\hbar v_{\mathrm{F}}|k| \tag{2}$$

where $s = +1$ for the CB and -1 for the VB, $\hbar$ is the reduced Planck's constant, $\mathrm{v_F} = 10^6$ m/s is the Fermi velocity of carriers in graphene, and $|\mathrm{k}| = \sqrt{\mathrm{k_x^2} + \mathrm{k_y^2}}$ is the wave vector of carriers in the 2D plane of the graphene sheet. The number of available electronic states *N*, in 2-dimensional k-space is given by

$$N = g_{\mathrm{s}} g_{\mathrm{v}} \frac{\pi k^2}{\left(\frac{2\pi}{L}\right)^2} \tag{3}$$

where $g_{\mathrm{s}} = 2$ is due to the fact that each k point has a degenerated double spin, and $g_{\mathrm{v}} = 2$ stems from the two valley degeneracy of the first BZ in graphene. Deviations from the conical band structure are not taken into account because most of the carriers of practical interest reside in the linear region of the dispersion curve. Using Eq. (2) and (3), an expression for the density of states *D(E)* (number of states per unit area per unit energy range) can be obtained as

$$D(E) = \frac{1}{A}\frac{dN}{dE} = \frac{2}{\pi}\frac{|E|}{(\hbar v_{\mathrm{F}})^2} \tag{4}$$

where the area $A=L^2$ has been used. Now we are in a position to evaluate the intrinsic electron density in graphene as

$$n = \int_0^\infty dE D(E) f(E) \tag{5}$$

where $f(E)$ is the Fermi-Dirac distribution function given by

$$f(E) = \left[1 + \exp\left(\frac{E - E_{\mathrm{F}}}{k_{\mathrm{B}} T}\right)\right]^{-1} \tag{6}$$

where k_{B} is the Boltzmann constant, T the absolute temperature, and $\mathrm{E_F}$ the Fermi level. The point$|\mathrm{k}| = 0$, called the "Dirac point," is a practical choice for the standard energy; thus, $E(|k = 0|) = 0$ eV. For intrinsic graphene, the Fermi level is unique, and moreover, it is located exactly at the Dirac point, $E_{\mathrm{F}} = 0$ eV. Then, the intrinsic carrier concentration in 2D graphene can be evaluated to a most approximate value as [36]

$$n_{\mathrm{i}} = p_{\mathrm{i}} = \frac{\pi}{6}\left(\frac{k_{\mathrm{B}} T}{\hbar v_{\mathrm{F}}}\right)^2 \tag{7}$$

At room temperature, the intrinsic electron and hole sheet densities can be estimated to be $n_{\mathrm{i}} \sim 9.81 \times 10^{14}\ m^{-2}$.

Next, we proceed to evaluate the carrier density originating from the gate bias and quantum capacitance [36, 37]. The presence of an additional series capacitance that exists in two-

dimensional (or one-dimensional) transistors with typical electrostatic capacitances of oxides is called the quantum capacitance. For low density of states (2D), quantum capacitance is important. In a grounded metal plate, the electric field from quasistatic charges is completely protected from penetration to the other side of the plate. In 2D system the electric field can partially penetrate the plate [38]. This gives rise to the concept of a quantum capacitance to account for the phenomenon. In general, the position dependent quantum capacitance in the graphene channel is expressed as $C_q(x) = -dQ_c(x)/dV_c(x)$, where $Q_c(x) = q\rho_s(x)$ is the sheet charge density and $V_c(x)$ the local electrostatic potential at any point *x* in the graphene channel. Using the standard procedure as in the case of intrinsic charge, $Q_c(x)$ can be obtained as

$$Q_c(x) = q\rho_s(x) = q\{p(x) - n(x)\} = q\frac{2}{\pi(\hbar v_F)^2}\int_0^\infty E\left\{\frac{1}{1+\exp\left[\frac{E+E_F(x)}{k_B T}\right]} - \frac{1}{1+\exp\left[\frac{E-E_F(x)}{k_B T}\right]}\right\}dE \quad (8)$$

where $n(x)$ and $p(x)$ stand for electron and hole sheet densities respectively. Noting that the gate voltage shifts the Fermi level in graphene and generates the channel voltage $V_c(x)$, we can write $E_F(x) = qV_c(x)$. Substituting this, an expression for the quantum capacitance can be derived from Eq. (8) as

$$C_q(x) = \frac{2q^2}{\pi}\frac{k_B T}{(\hbar v_F)^2}\ln\left[2\left\{1+\cosh\left(\frac{qV_c(x)}{k_B T}\right)\right\}\right] \quad (9)$$

Since the electrostatic capacitances and the quantum capacitance act in unison to generate the carriers we combine them in a capacitive circuit as shown in Fig. 2, from where $V_c(x)$, the potential attached with the quantum capacitance, may be expressed as:

$$V_c(x) = (V_{GSt-eff} - V(x))\frac{C_t}{C_t + C_b + \frac{1}{2}C_q(x)} + (V_{GSb-eff} - V(x))\frac{C_b}{C_t + C_b + \frac{1}{2}C_q(x)} \quad (10)$$

where C_t and C_b are the top and back gate oxide capacitances respectively, and $V_{GSt-eff}$ and $V_{GSb-eff}$ are the effective values (explained below) of the gate to source top and back gate voltages respectively; $V(x)$ stands for the net electrostatic potential in the channel at the point under consideration.

As far as chemical doping is concerned, it is potentially challenging due to the sp^2 bond. Although there are some preliminary successes, these are primarily meant for inducing band gap rather than enhancing the carrier density [39]. If real doping will be possible, the dopant density will determine the carrier density, as in semiconductors.

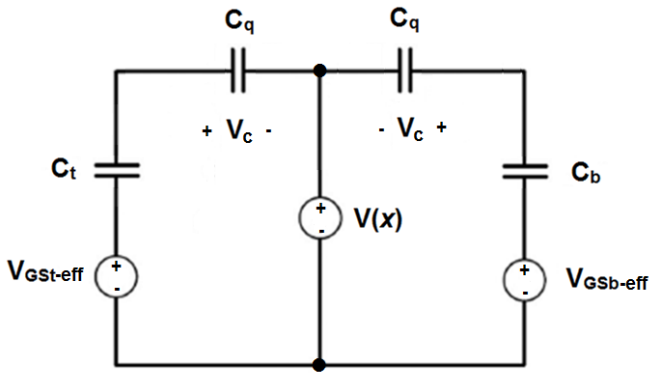


Figure 2. Capacitive circuit for the GFET, the + and – signs only indicate higher and lower (magnitude) ends of the potentials.

The carrier velocity can be modeled as [40, 41]

$$v(x) = \frac{\mu \mathcal{E}(x)}{\left[1 + \left\{\frac{\mu \mathcal{E}(x)}{v_{\text{sat}}(x)}\right\}^{m}\right]^{1/m}} \tag{11}$$

where, $\mathcal{E}(x)$ is the electric field, μ is the carrier low-field mobility, and v_{sat} is the saturation velocity. Different authors use different values for m to fit their results with experimental data; in this work we have chosen $m = 1$. The saturation velocity at high carrier density simplifies to [40]

$$v_{\text{sat}}(x) = \frac{2}{\pi} \frac{\omega_{\text{op}}}{\sqrt{\pi \rho_{\text{s}}(x)}} \tag{12}$$

where, $\hbar\omega_{\text{op}}$ is the optical phonon energy. Following the standard approach described above (also Ref. [42]), we have proposed a quasi-analytical model for graphene field effect transistors. The GFET modeling approach then boils down to Eq. (1) which can be integrated, with the change of parameters, to obtain a final expression for the drain current I_{DS}. Applying $\mathcal{E}(x) = -dV(x)/dx$, and substituting v(x) from Eq. (11) into Eq. (1) and integrating over the channel length L, the drain current is obtained as:

$$I_{\text{DS}} = q\mu W \frac{\int_0^{V_{\text{DS-eff}}} \rho_s(x)\, dV(x)}{L - \mu \int_0^{V_{\text{DS-eff}}} \frac{dV(x)}{v_{\text{sat}}(x)}} \tag{13}$$

where $V_{\text{DS-eff}}$ stands for the effective value (explained below) of the applied drain to source voltage.

The simulation process starts with dividing the channel length into a suitable number of space steps in the x-direction. The properties of the channel are assumed uniform in the y-direction. The simulation aims at determining $\rho_{\text{s}}(x)$ and $v(x)$ at each space step starting from the source end to the drain end of the channel. $\rho_{\text{s}}(x)$ could be determined using Eq. (8), but it has one unknown parameter $E_{\text{F}}(x) = qV_{\text{c}}(x)$. In an attempt to determine $V_{\text{c}}(x)$ using Eq. (10) it is noted that it involves $\text{C}_{\text{q}}(\text{x})$. Although $\text{C}_{\text{q}}(\text{x})$ is determinable using Eq. (9), the presence of $\text{V}_{\text{c}}(\text{x})$ in the equation does not permit a straightforward solution. The way out is therefore, to solve Eqs. (9)

and (10) simultaneously in a self consistent manner to determine $C_q(x)$ and $V_c(x)$ together. Then $\rho_s(x)$ is determined either using Eq. (8) or the following equivalent relation:

$$\rho_s(x) = \left| -\frac{1}{2q} C_q(x) V_c(x) \right| \tag{14}$$

A realistic simulation method should incorporate the effect of several other factors such as (i) the work function difference between the gate and graphene channel, (ii) the charged impurities of the oxide which cling to the graphene surface and those which have image in graphene and (iii) the intentional or unintentional doping of the graphene channel. These factors contribute to the potential and hence the sheet carrier density in the channel. The effects of all these factors are taken into account by replacing the applied gate voltages with their effective values:

$$V_{t-eff} = V_t - V_{t0}, \qquad V_{b-eff} = V_b - V_{b0} \tag{15}$$

where V_t and V_b are the applied top and back gate voltages respectively, and V_{t0} corresponds to the top gate voltage at the Dirac point (that signifies the minimum carrier sheet density) with zero applied back gate and drain-source voltages. A similar definition for V_{b0} is used to determine its value.

The source and drain contacts introduce some resistances. Part of the applied drain bias drops across these resistances. So, the actual drain voltage is less than the externally applied bias. This is taken into account by introducing an effective value for the drain to source bias $V_{DS\text{-}eff}$ in the following way:

$$V_{DS-eff} = V_{DS} - I_{DS}(R_S + R_D) \tag{16}$$

where V_{DS} is the externally applied drain to source voltage, R_S and R_D are the source and drain contact resistances respectively. But the value of drain current I_{DS} involved in Eq. (16) is not yet determined. In order to alleviate the situation, we have formulated an iteration technique which iterates over an initial input trial value of the drain current, and determines the output drain current following the simulation method described above using the effective value of drain to source voltage from Eq. (16). If the input and output drain currents do not match, then the input current is varied in a controlled manner and the process is repeated until the two values converge. The source contact resistance also affects the values of the gate voltages that appear at the channel. This is taken care of in a similar manner and the gate to source effective top and back gate voltages are estimated as

$$V_{GSt-eff} = V_{t-eff} - I_{DS} R_S, \qquad V_{GSb-eff} = V_{b-eff} - I_{DS} R_S \tag{17}$$

Based on the process described above we have developed a simulation software on the MATLAB platform and we have used the same for the present work. The program software has been developed in such a way that it is free from any numerical instability and consumes less computation time while at the same time it takes care of a reasonable degree of computational accuracy.

4. RESULTS AND DISCUSSION

One of the most pioneering work on experimental GFET is due to Meric et al. [29]. Because of the widely acclaimed results, we have considered the work for the validation purpose of our simulation method. Accordingly, we designed a GFET with the same structural parameters as in [29] which are also presented in Table 2. The top- and back-gate dielectric materials are chosen as HfO_2 and SiO_2 respectively in accordance with those of [29] (this has been designated as G5 in Table 1). The output characteristics of the GFET structure are computed from our simulation method and are compared with those of [29] in Figure 3(a). Interestingly, we obtained an excellent agreement. This is not only a testimony to our modelling approach but also it vindicates the simulation method that we have adopted. Additionally, our simulated transfer characteristics shown in Figure 3(b), when compared with those of Thiele et al. [42, Figure 5(b) therein], have the best overall general agreement (minor deviations are due to choice of different R_S and R_D in the two cases), further corroborating with the simulation approach followed here.

Table 2 Parameters as in the experimental report [29]

Parameters	Value
Top-gate dielectric thickness (t_{top})	15 nm
Back-gate dielectric thickness (t_{back})	285 nm
Channel length (L)	1 μm
Channel width (W)	2.1 μm
Back-gate bias (V_b)	-40 V
Optical phonon energy ($\hbar\omega_{op}$)	55 meV
Minimum sheet carrier density (ρ_{s0})	1.5×10^{16} m^{-2}
Source contact resistance (R_S)	1100 Ω
Drain contact resistance (R_D)	300 Ω

Our validated simulation method has been employed to characterise the GFET structures of Table 1 with a view to unveil some new features. To begin with, we computed the transfer characteristics. The plots are presented in Figure 4(a) at V_{DS} = -1 V and V_b = -40 V. While the nature of the curves remains the same, the curves undergo a systematic elevation in the current scale from structure G2 to G6. The current value increase with increasing ε_r, with the later in fact making a greater contribution to the sheet carrier density due to an increase in gate capacitance, precisely explains the observed characteristics. In fact, such an observation has set forth sufficient scope to engineer the I~V characteristics of GFETs by tailoring the gate dielectric material. It is further observed from Figure 4(a) that the Dirac point is progressively left shifted with increase in the value of top-gate ε_r. However, the scenario takes a U-turn in Figure 4(b) when the back-gate voltage becomes positive, V_b = +40 V.

The curves as well as the Dirac points are now right shifted (towards higher V_t with increase in ε_r; elevation in the current scale however is retained. This is a clear manifestation of the ambipolar nature of graphene [32] which in turn is reminiscent of the fact that the ambipolar characteristics can be suitably engineered with an ingenious choice of the dielectric material. The output characteristics of the GFET structures G2 to G6 are studied for different combinations of V_t and V_b and the results are shown in Figure 5 (a) through (d).

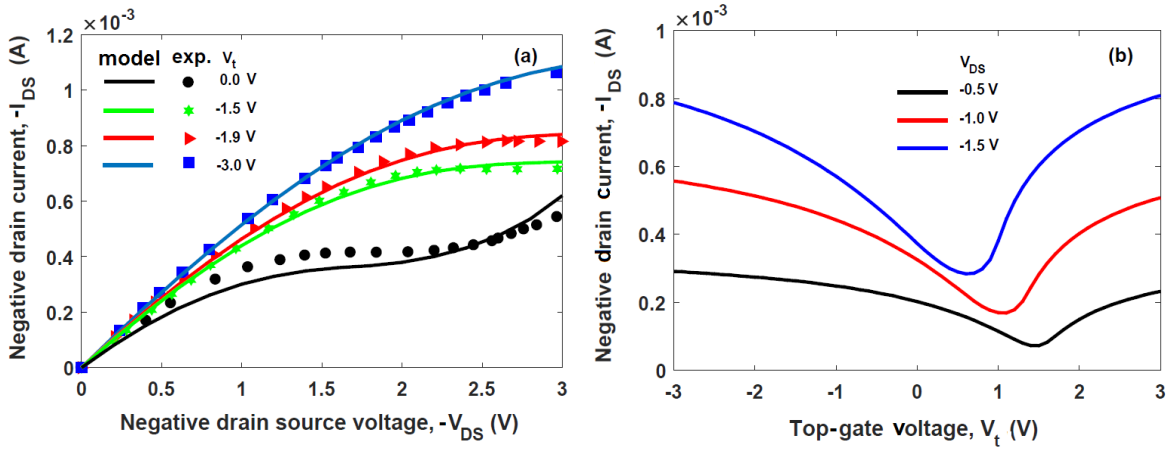


Figure 3 (a) Simulated output characteristics of G5 and comparison with experimental data from Ref. [29], (b) Simulated transfer characteristics of G5 for comparison with Ref. [42, Figure 5(b)].

Figure 5(a) plotted for V_t = -1 V and Vb = -40 V reveals the expected feature of drain current enhancement with rise in top-gate ε_r. The presence of the characteristic kink is also observed from the figure but for restricted cases such as high ε_r and higher value of drain voltage. It is worth to mention here that the kink effect in the I~V characteristics of GFETs results in the possibility of crossover among the curves giving rise to zero or negative transconductance which is highly detrimental for analog applications [14]. Since the kink effect is absent for GFETs with $\varepsilon_r \leq 10$ and for $V_{DS} \leq 3$ V, such GFETs may prove to be highly suitable for analog devices.

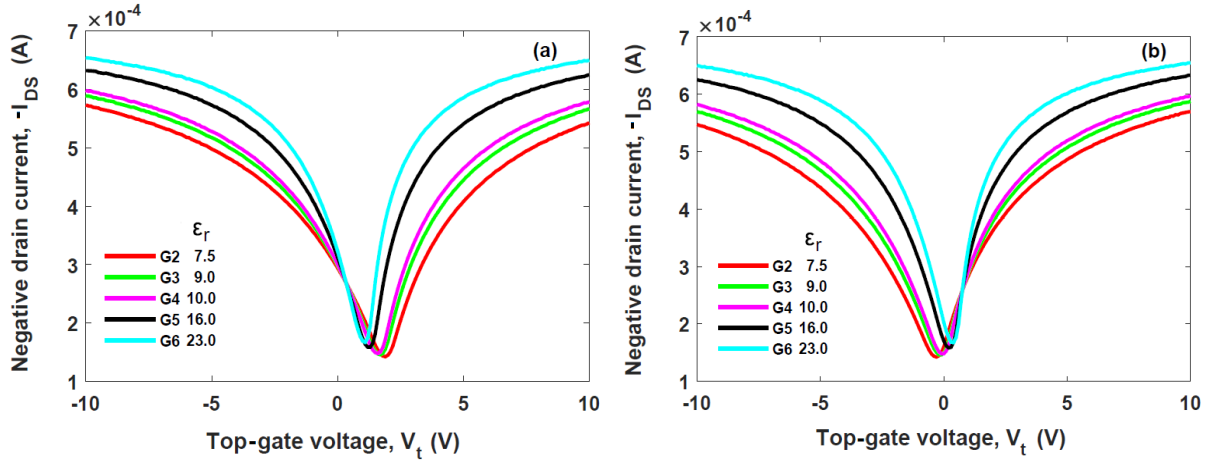


Figure 4 Transfer characteristics of the GFET structures G2 to G6, the corresponding top-gate dielectric constants for the structures are shown in the legend, (a) at V_{DS} = -1 V and V_b = -40 V , (b) at V_{DS} = -1 V and V_b = +40 V.

The output characteristics computed for V_t = -1 V and V_b = +40 V are shown in Figure 5(b). All the curves are marked by the kink effect. So, unless there is a special purpose device requirement, this combination of gate voltages should be avoided for analog domain in whatsoever dielectric material is used for the top-gate. Now coming to Figure 5(c), we notice that the nature of the curves has completely changed when V_t = +1 V and V_b = -40 V.

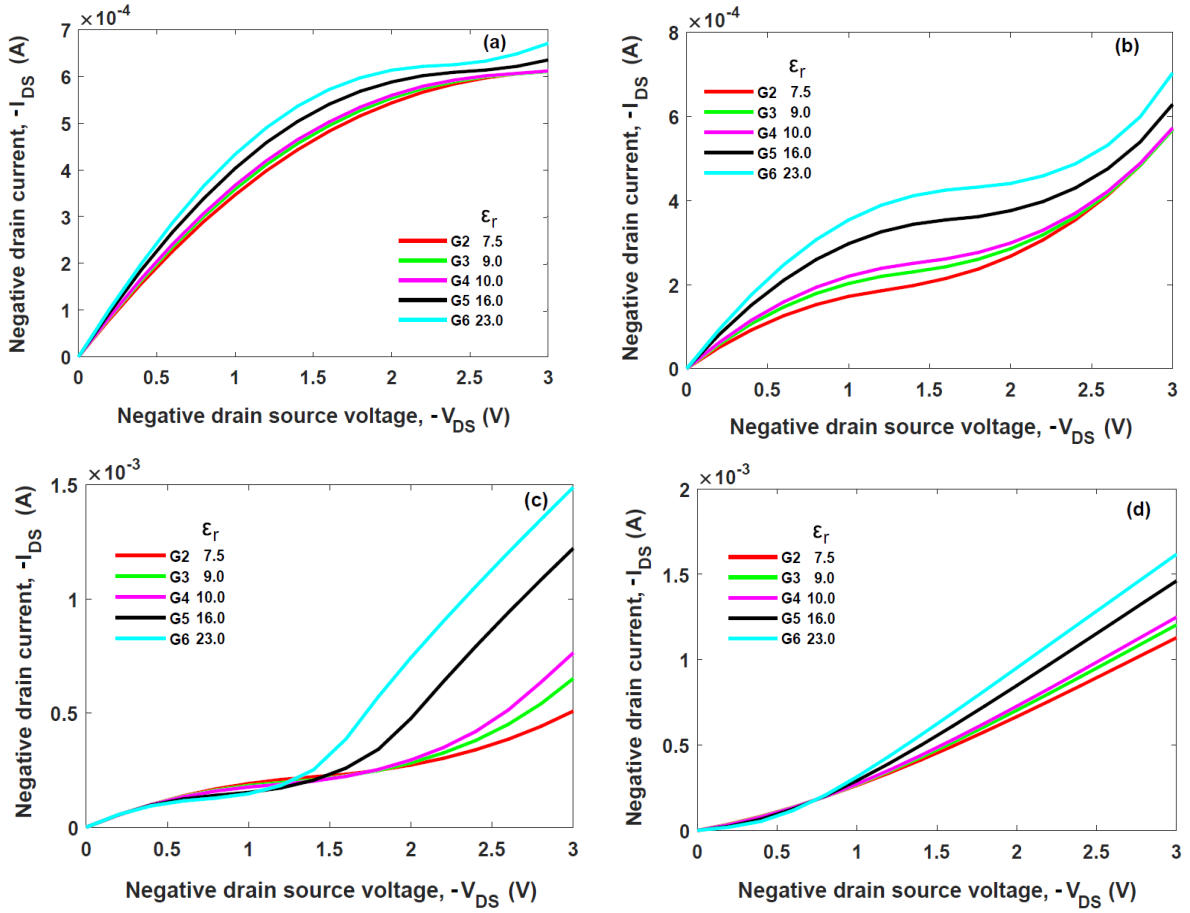


Figure 5 Output characteristics of the GFETs from G2 to G6, (a) at V_t = -1 V and V_b = −40 V, (b) at V_t = −1 V and V_b = +40 V, (c) at V_t = +1 V and V_b = −40 V, (d) at V_t = +1 V and V_b = +40 V.

The output characteristic of each GFET is now marked by a point of inflexion which shifts towards lower magnitude of V_{DS} as the ε_r rises from structure G2 to G6. Further, the drain current rises distinctly beyond the point of inflexion and the rise becomes steeper with increase in ε_r. These are some novel features of the output characteristics with a lot of potentials for novel applications in such diverse areas as power electronics and switching [43]. The output characteristics for the final combination of applied gate voltages, V_t = +1 V and V_b = +40 V, are shown in Figure 5(d). While the curves have more or less similar features as in Figure 5(c), a testimonial convergence of the points of inflexion for all the GFETs from G2 to G6 with different ε_r is interesting. Potential applications of such observations are still lacking.

We also investigated the effect of top-gate dielectric thickness on the output as well as transfer characteristics of GFETs. We choose the gate dielectric material as in G5 because this is a practical structure fabricated in Ref. [29] and it has set a benchmark in GFET standard. So, we chose G5 and varied the top-gate thickness (t_{top}) from 15 to 35 nm. Figure 6(a) shows the plots of transfer characteristics of the GFETs with varying top-gate dielectric thickness at V_{DS} = -1 V and V_b = -40 V. With increase in t_{top}, not only the overall current decreases but also the curves are right-shifted including the Dirac points. It is interesting to note that such observation is just the opposite of what we observed for the case of increase in ε_r (Figure 4(a)). This is a natural consequence of the reflective impact of the top-gate capacitance (C_t) on the channel carrier density which is directly proportional to ε_r but varies inversely with t_{top} [1], stated in Eq. (18) below for clarity,

$$\rho_s = \varepsilon_0 \varepsilon_r V_t / t_{top} q \qquad (18)$$

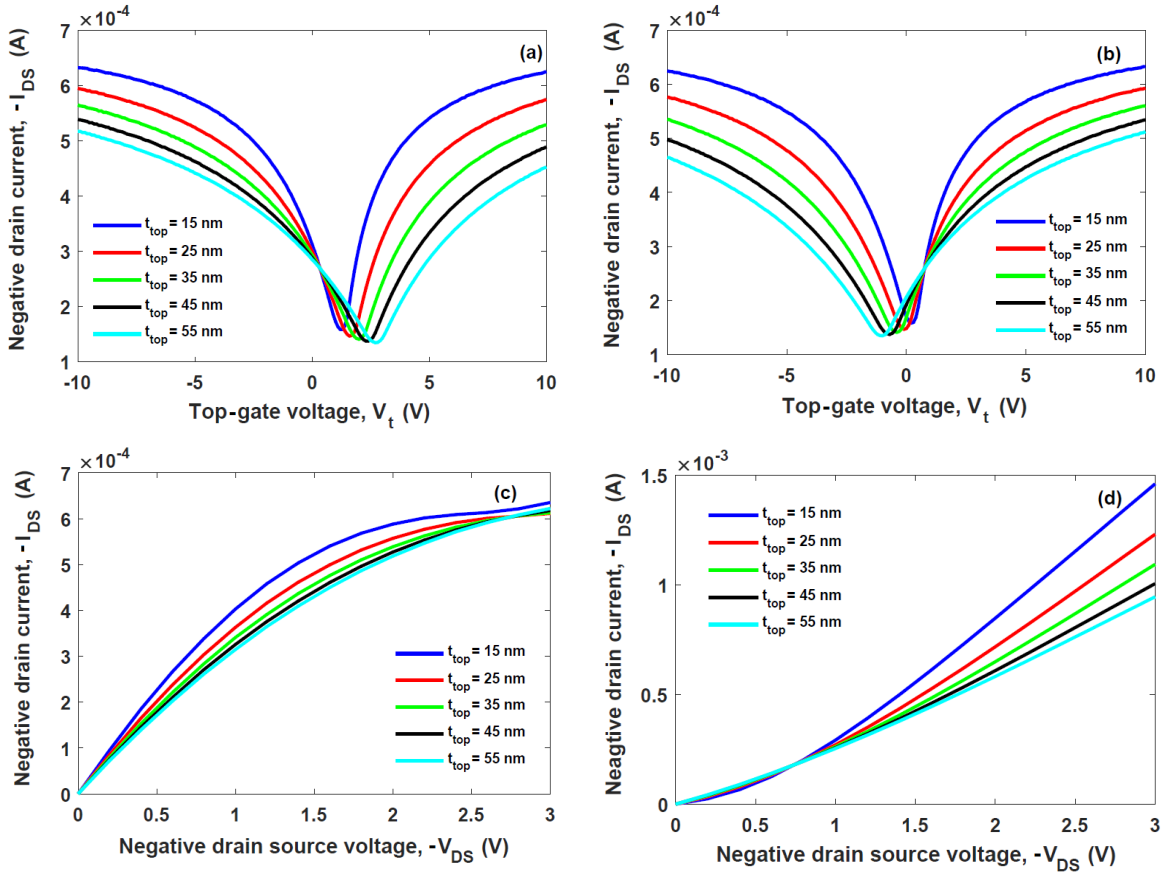


Figure 6. Effect of top-gate thickness, (a) on transfer characteristics of G5 at $V_{DS} = -1$ V and $V_b = -40$ V, (b) on transfer characteristics of G5 at $V_{DS} = -1$ V and $V_b = +40$ V, (c) on output characteristics of G5 at $V_t = -1$ V and $V_b = -40$ V (d) on output characteristics of G5 at $V_t = +1$ V and $V_b = +40$ V, .

Nonetheless, the trend in left-right shifting of the curve as well as the Dirac point is strongly influenced by the back-gate voltage (V_b). Therefore when V_b is changed from -40 V to +40 V, we noticed a reverse shift in the curve and the Dirac point (Figure 6(b)). For reason stated earlier, this trend is also opposite to the trend in Figure 4(b). The top-gate thickness effect on output characteristics is shown in Figure 6(c) at V_t = -1 V and V_b = -40 V. The curves with higher thickness suffer less from the characteristic kink effect but a crossover is imminent beyond V_{DS} = 2.5 V. Although higher thickness leads to a lower current, a better current saturation characteristic may be considered as a silver lining for the analog domain. When both the gates are made positive (V_t = +1 V and V_b = +40 V), we get the output characteristics as in Figure 6(d). Comparing with Figure 5(d), we notice a reverse trend with regard to the respective parameters, in the two cases, for reasons already stated. Finally, convergence of the inflexion points emerges as a new feature of the positive dual-gated GFET.

To investigate further into the top-gate thickness dependence on the current characteristics of the GFETs, a plot of the drain current as a function of $1/\ t_{top}$ is shown in Figure 7(a) for all the GFET structures G1 to G6 listed in Table 1 for a wide range of t_{top} from 10 to 400 nm. From these curves three features are evident two of which are already discussed above namely increase in current with ε_r and decrease with t_{top}. The third and the interesting feature is the widely varying slopes of the GFETs from G1 to G6 particularly when the thickness is high. As a result, at higher values of top-gate thickness (t_{top} > 400 nm), it seems all the GFETs tend towards nearly the same value of the drain current (-0.25 mA in Figure 7(a)), irrespective of the different top-gate dielectric materials. So GFETs with very high value of the top-gate thickness will be relatively numb to the type of dielectric material chosen.

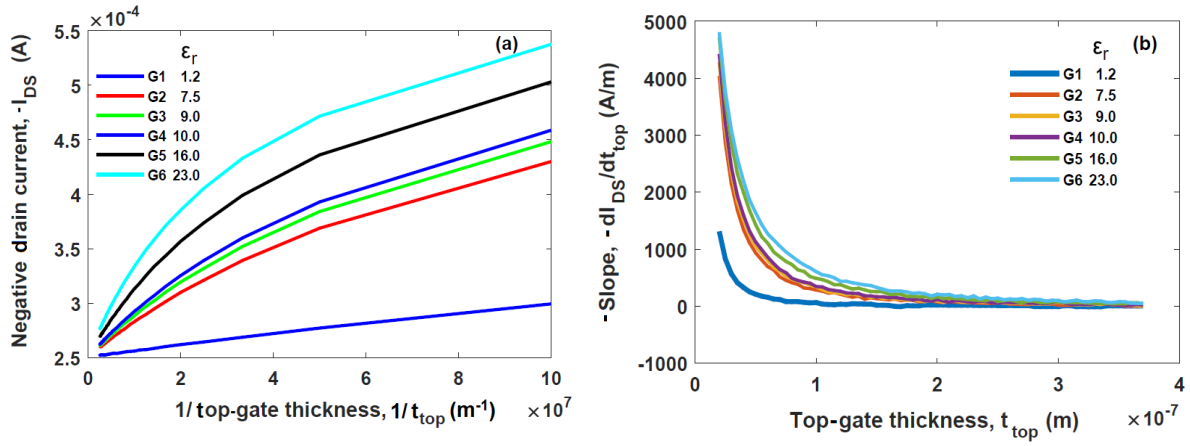


Figure 7. (a) drain current characteristics as a function of the reciprocal of top-gate dielectric thickness, (b) rate of change of current with respect to top gate dielectric thickness.

To explore further into the process of drain current variation with t_{top}, we have plotted the slope of the I_{DS} versus t_{top} curves ($-dI_{DS}/dt_{top}$) in Figure 7(b). GFETs with higher ε_r are associated with sharper gradients at the lower side of t_{top}. The slope maxima recorded in Table 3 stand additional testimony to this fact. But as the top-gate thickness increases, the gradient considerably reduces in each case of the top-gate dielectric and ultimately tends towards the zero slopes asymptotically, keeping hardly any distinction among the dielectric materials. To curb out the asymptotic nature of the slopes, we define a figure of merit named "critical thickness" (of the top-gate dielectric) as the thickness when the slope reduces to ~100. Taking the maxima of the slopes into account, a slope of 100 can be considered very small ($\cong 0$). So the critical thickness is a measure of the top-gate thickness corresponding to $dI_{DS}/dt_{top} \cong 0$. In other words it is that thickness beyond which the current saturates with respect to increase in t_{top}. The values of the critical thickness for GFETs with different top-gate dielectrics are shown in Table 3. GFETs with lower ε_r have a smaller critical thickness. This is indicative of the fact that top-gate dielectric like SiO_2 ($\varepsilon_r = 3.9$) will be unaffected by increase in thickness beyond ~150 nm where as ZrO_2 will exhibit thickness induced current variation up to ~350 nm. While higher ε_r enhances the drain current, it suffers from delicate thickness sensitivity. But at the same time, the latter can lead to new potential applications.

Table 3 Slope parameters of the drain current characteristics with respect to top-gate thickness

GFET structure	Top-gate dielectric constant (ε_r)	Negative maximum slope $-(dI_{DS}/dt_{top})_{max}$	Critical thickness at $-(dI_{DS}/dt_{top})$~100
G1	1.2	1314.5	90 nm
G2	7.5	4042.0	230 nm
G3	9.0	4279.8	245 nm
G4	10.0	4427.6	265 nm
G5	16.0	4719.2	305 nm
G6	23.0	4808.3	365 nm

5. CONCLUSION

Gate dielectric material has a significant impact on the performance of a GFET. The choice of a dielectric material and its dimension for any desired GFET characteristics has been the focus of this study. A well-defined computer simulation method developed by us and described in Sec 3,

has been employed for this purpose. The results from GFETs with different gate dielectric materials establish the importance of careful consideration of gate dielectric materials for optimization of GFET characteristics. As expected, the results confirm that the ambipolar characteristics can be engineered with suitable dielectric material and dimensions. The shifts in Dirac point as well as the inflection point can be modelled as a function of ε_r. A testimonial convergence of all inflection points in the output characteristics of the GFET at top-gate voltage of +1 V and back-gate potential of +40 V, for different gate dielectric materials, is exciting. It is further interesting to note that the drain current saturates after a certain critical thickness and that such thickness is more for higher ε_r. In addition, this study will bear a significant importance to choose the suitability of a given set of structural and operating parameters to envisage a GFET for application in analog as well as digital domains.

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