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The Effect of Embedding a Thin Layer of a Polymer on Resistive Switching Characteristics for Au/CdSe/Au Structure

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ABSTRACT

The phenomena of resistance random access memory (RRAM) depending on the altering of resistance between at least two values has been found in materials such as transition metal oxides, some semiconductors or insulators materials, named as resistive switching. The developments on RRAM have been started due to its low power consumption, simple structure, high-density, high – speed resistive switching, impressive retention with small-feature size. Regardless of the wide-ranging research, basic switching conduction mechanisms of the resistive memory structures are basically depending on the certain special materials. To improve the current structure performance, the Cellulose Acetate as a polymer was added to the active layer (cadmium selenide CdSe). The polymer material was used to form the second active coating to construct the Au/CdSe/polymer/Au as new structure. This material may enhance the cell performance by increasing the charges traps. This procedure leads to increasing resistance ratio (Rratio) and decreasing the working voltages of structure. A spin coating apparatus was used to coating the polymer layer on CdSe. The glass was used as a substrate and the first active layer deposited under vacuum by thermal evaporating system. The cell was sandwiched between the two electrodes in the same materials (Au) which deposited also under the same system. Bipolar resistive switch, in this memory structure, is observed in its switching operation. The zone of the upper electrode (Au) has a significant affect upon the resistive performance. This influence is became further in the big upper electrode zone (TEL=13.5mm2) where the high-resistance (HRS) are inversely related to the upper electrode zone (A). This occurs inducing more traps in case TEL (hanging sentence). Finally, the (Rratio) is directly proportional with the electrode zone (A). The compliance current (Icc=30mA) are used for protecting the structure from the damage. The current structure has many properties, such as Vset = 3.9V, VReset = -1.9V and Rratio about 176 in case of TEL. We conclude from this research that the embedment of a thin layer of a polymer which have been used in this research are improving the high density, enhancing high speed with low cost as well.

Keywords: Resistive Switching in CdSe Layers, ReRAM Memory, Bipolar RS Structure, Resistive Switching in Polymer, Non-Volatile Memories.

1. INTRODUCTION

Switching phenomena have already received a lot of attention because of their promising new applications in non-volatile memory emerging technologies of the next generation, as conventional flash memory quickly approaches its own fundamental scaling limitation due to the rising difficulty of retaining electrons in reduced dimensions [1].

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All memory devices divided into two groups, volatile and non-volatile. Both of these kinds of memory are complementary to the CMOS technology. Thus, MOS memory is also divided into many groups of other storage devices based upon the storage type and the access time [2].

The resistive switching features of different materials, resistive switching mechanisms and suitable methods of enhancing resistive switching properties have already been investigated for potential future non- volatile memory applications [3].

Organic materials have already attracted significant interest in the manufacture of memory devices capable of reversibly switching between two states, always commonly referred to as the "0" and "1". In organic materials, both states can be controlled by voltage or current to exhibit high or low resistance. Polymer memory devices have the potential to display non - volatility features. This means that they allow low standby power operation and save energy. In addition, polymer microelectronics is cheaper to manufacture for storage of information than silicone-based devices [4].

Cadmium selenide CdSe is a direct band gap semiconductor (Eg = 1·7 eV) belonging to the II–VI groups. Many physical and chemical methods are existed for the growth of CdSe thin films. A large number of methods to coat or deposit CdSe films were used out of which the electron beam evaporation method, one of the physical vapor deposition methods, has been commonly used for the growth of structure quality thin films CdSe films have been grown by vacuum evaporation system and employed as gas sensors for the detection of oxygen [5].

Kaur *et al*, showed that CdSe/PVP nano-composite (NC) has been synthesized by employing Polyvinyl-pyrrolidone (PVP) as a polymer matrix. The chemical technique using PVP as a polymer matrix has produced CdSe / PVP nanocomposite. XRD has been used for verifying the crystallinity of the CdSe/PVP NC with zinc blende structure. The spherical nature, of CdSe nanoparticles with element size from 4 to 5 nm, is displayed in the TEM test. The mean crystallite size computed from XRD model is 4.38 nm, and that is in excellent fitting with TEM results. The structure with added PVP film represents good retention capacity caused by the repressed tunnelling of charge carriers from the nano-particles to the electrodes. The conductivity switching mechanism of the CdSe/PVP NC structure has been studied by Current–Voltage (I–V) and Capacitance–Voltage (C–V) testing. I–V and C–V properties reveal hysteresis behavior caused by the charge trapping and detrapping in the CdSe nano-particles. Good reliability and stability of the structures have been verified from the retention properties [6].

Di Wu, T. Xu and et al., summarized the mechanisms involved of n-CdSe RS memory are very well defined and recognized by electrons trapping and detrapping within the interface oxide layer. i.e., when a forward voltage signal is applied, CdSe electrons are injected into the interface oxide layer and trapped by oxygen vacancies within the interface oxide layer. This process can decrease the depletion layer width and trigger the ON memory status. On the contrary, under reverse voltage, the trapped electrons are going to be released and come back to CdSe , which is able to cause the OFF state [7].D. Hu, G. Zhang and et al., work provided a high - performance non-volatile memory device using CdSe as quantum dots (QDs) composites in NVM with impressive retention features and a large memory window at low programming voltage. Trapped electrons and holes, within the QDs, regulated the electrical performance and holes within the QDs. QDs have been used as trap centers for holes and electrons [8].

However in the case of a non- volatile information storing device relayed on hybrid Nano composites, the memory effect is strongly associated with the existence of inorganic nanoparticles (NMs), such as that of ZnO QDs, Au NPs, CdSe NPs and CNTs, which are integrated in a polymer matrix because the current difference between the ON and the OFF states for the polymer- only device is insignificant[9].

Multi-level three-state resistive memory structures were constructed using CdSe/ZnS quantum dots (QDs) and ZnO nano-particles (NPs). Poly-vinyl carbazole (PVK) was additional to the synthesized CdSe/ZnS QDs with a core/shell structure to create sturdier charge storage film in the QDs. The usage of PVK aids the design-stage control of the state current and write voltage, along with development of the Rratio= RHRS/RLRS. All thin layers were constructed by the solution spin coating technique. Added quantum wells can be formed using ZnO NPs, which allows the multistate working. We improved the process conditions with respect to PVK and ZnO NPs, and confirmed that the PVK concentration was improved at 2.5 wt%. The constructed structure revealed high stability and reliability through 20 repeat cycles, and showed a retention time of 80 h [10].

In general, that is lacking in some above memories, so in the current research has been used some a polymers such as Cellulose Acetate were embedding to the CdSe as active layer to improve some memory parameters such as the resistance ratio (Rratio=RHRS/RLRS) by increasing this rating as possible and decreasing the working voltages (Vset and VReset) as possible.

2. METHODOLOGY

To create the current structure (after embedding the thin film of a polymer), a glass slides with (25mm ×75mm) are used as a substrate and prepared using a distinct washing process. After washing and cleaning the substrate, a thin layer of gold (Au) with thickness (3000Å) are depositing as a lowest electrode by using the thermal vaporization system (the Balzer system). Using the same thermal vaporization system, a thin layer of Cadmium Selenide CdSe was deposited on the (Au) with thickness (750Å). Here, the CdSe thin film is active material and represents the n-type semiconductor.

CdSe is optical material and affected with the light (photo-effects) [11] because the optical measurements show that the CdSe thin films have direct band gap [12]. Before the ending step, the spin - coater apparatus category (INSTRAS, sck-100 spin coater kit) are used to coating a thin layer of a polymer (Cellulose Acetate) on the CdSe layer with thickness about 1000Å. Finally, to complete the construction of the structure, a thin layer of metal (Au) with thickness of (3000Å) were deposited as upper Electrodes (TE) for three zones (13.5 mm2, 3.5 mm2 and 2.3 mm2) on the thin layer of a polymer (see figure 1). The structure was checked with dc source using maximum current of (Icc= 20 mA) as a compliance current to protected the structure from damage.

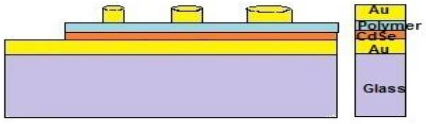

Figure 1. The cross section of the structure after embedding the thin film of a polymer.

3. RESULTS AND DISCUSSION

3.1 Testing the Devices using DC Measurements

The dc checking of structure can be accomplished by using (I-V) properties of the constructed structures were determined by (KEITHLEY 6487 PICOAMMETER / VOLTAGE SOURCE) for three cases and without exposed this structure to the light as possible (using a cover about the structure):

i. In case of big upper Electrode (TE_L), the zone is AL= 13.5mm^2.
ii. In case of medium upper Electrode (TE_m), the zone is A_m= 3.5 mm^2.
iii. In case of small upper Electrode (TE_S), the zone is A_S= 2.3 mm^2.

By way of the result of dc (I-V) properties, Figure 2 shows the relationship between the I and V for structure without embedding a thin layer of a polymer by taking three different electrodes zones (TE_L, TE_m and TE_s).

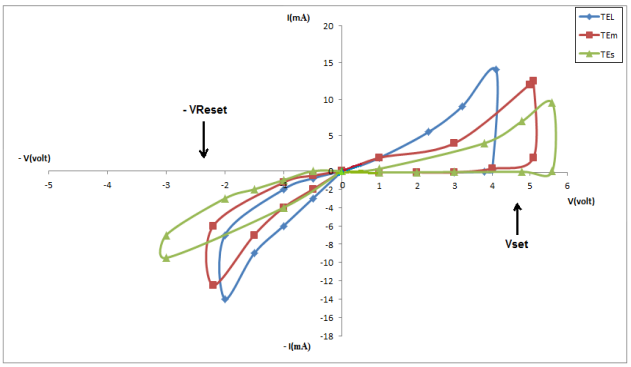

Figure 2. Properties of the structure for many electrodes zones without embedding a thin layer of a polymer using compliance current I_{cc} = 30mA.

From above figure, the effect of the upper electrode zone on the resistive switching behavior can be observed, but when embedding a thin layer of a polymer, the important properties of resistive switching for the percent structure was improved such as Vset and VReset ….ect. (See figure 3), so this structure is using as Schottky memory [13].

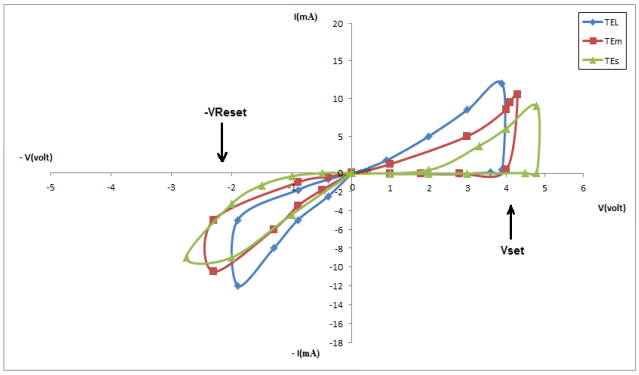

Figure 3. (I-V) properties of the structure for many electrodes zones after embedding a thin layer of a polymer using compliance current I_{cc} = 30mA.

From above figure, the values of voltages (Vset , VReset and low resistance switching (RLRS)) in case of TE_S will be higher than those values in case of TE_m and TE_L individually. But the resistance of the structure at high resistance switching (RHRS) case are inversely related with varying of the upper electrode zone, this case are corresponding with conclusions the investigator Seo and et al., for resistive switching [14]. To safety the structure from the damaging, a compliance current (I_{cc}) was used, so this equal to I_{cc}=20mA. The changing of this above values can be shows in table 1.

Table 1 shows the main measured values of the structure for the many Uppers electrodes zones

	TEL	**TEm**	**TES**
Vset	3.9V	4.3V	4.8V
V_{Reset}	- 1.9V	- 2.3V	- 2.75V
RHRS	27.8571KΩ	33.076KΩ	40KΩ
RLRS	0.1583KΩ	0.219KΩ	0.3055kΩ

The above curves revealed that the present structures are behaved as bipolar resistive switching. This behavior may depending on the conduction mechanism of CdSe material [11]. As mentioned above, the principle of Schottky memory can be easily recognized from the energy-band diagram illustrated in figure 4.

The interfacial layer (polymer) at the junction interface has a similar structure to the floating gate memory. The oxygen vacancies that grow out of a polymer 's internal composition will act as electron trapping centers. In the forward bias conditions, electrons from the CdSe are injected into the interfacial layer and trapped in the interfacial region by oxygen vacancies. This process decreases the height of the Schottky barrier and leads to the memory ON state (LRS) (figure 4(a)). That corresponds to a memory write operation.

In conversely, electrons trapped in the interfacial layer by oxygen vacancies are injected into CdSe under reverse bias conditions, resulting in an increase in the barrier height, that's leads to a memory OFF state (HRS), which is the memory erase process (Figure 4(b)) [13].

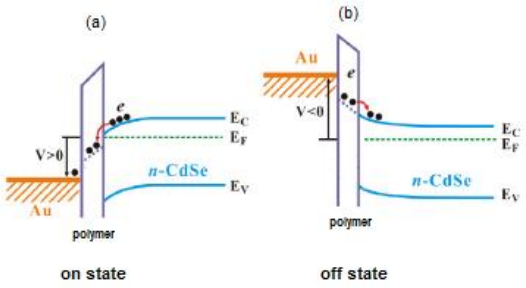

Figure 4. The energy-band diagram of the CdSe/polymer/Au Schottky memory in (a) the ON state and (b) the OFF state.

The most for all form of cellulose acetate fiber has an acetate group on approximately 2–2.5 of every three hydroxyls. This cellulose diacetate is recognized as secondary acetate, or simply as ‘‘acetate’’ [15] (See figure 5).

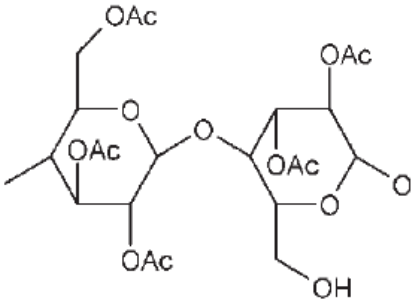

Figure 5. The chemical composition of the cellulose-2.5-acetates.

The chemical composition of the cellulose acetate (polymer) revealed it has, hydrogen, carbon, some internal impurity and oxygen, so this oxygen atoms can serve as the trapping centers for electrons.

From table 1, the resistance ratio (R_{ratio}= RHRS/RLRS) can be calculated for many upper electrodes zones and summarizing in table 2.

Table 2 Rratio of the structure for many uppers electrodes zones

R_{ratio}		
TEL	***TEm***	***TEs***
175.97	151.0319	130.932

From table 2, there are direct relation between A and Rratio for uppers electrodes zones of the structure as shown in fig 6.

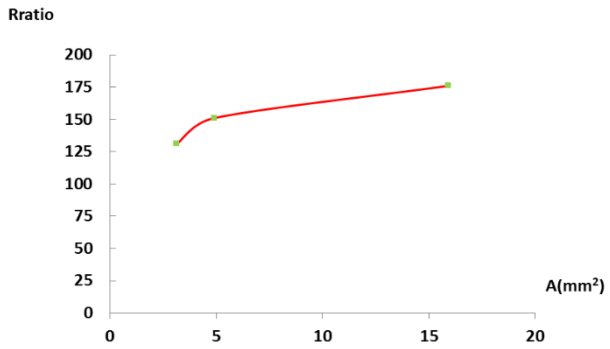

Figure 6. The relationship between A and Rratio for Uppers electrodes zones of the structure.

The resistor endurance (LRS and HRS) of the structure in case of TE_L, TE_m and TE_s were studied. This represented the number of cycles between the (ON) and (OFF) state or as named (Set/Reset cycles) which can be used for the memory before it has been permanently damaged [16], see figure (7). This figure shows about two orders of the value between high resistance state (HRS) and low resistance state (LRS) (the values LRS is in fractions KΩ and the values of HRS is in tenths KΩ).

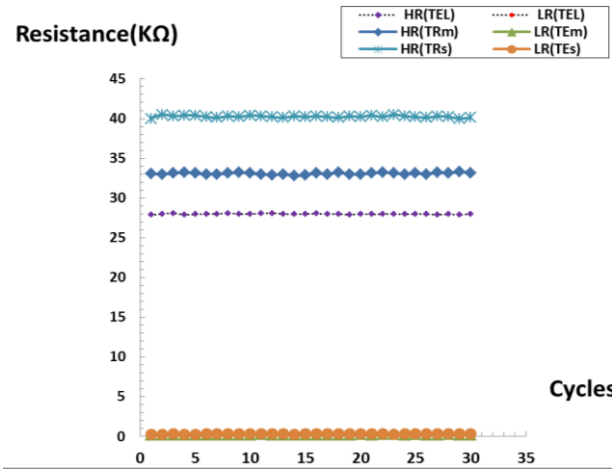

Figure 7. Endurance for resistance HRS and LRS of the structure in three cases of upper electrodes TEL, TEm and TEs.

Similarly, the voltage endurance (VReset and Vset) of structure in three cases of upper electrodes TE_L, TE_m and TE_s were studied, see figure (8).

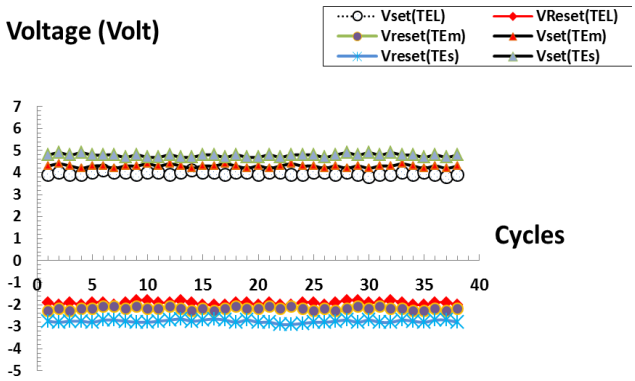

Figure 8. Endurance of the voltages (VReset and Vset) of the structure in three cases of upper electrodes TEL, TEm and TEs.

3.2 Testing the Device using AC Measurements

The ac checking of the structure can be accomplished, by using (I-V) characteristic of the constructed structure without exposed the structure to the light as possible. The measurements were achieved using storage digital oscilloscope category (OWON MSO 7102T) and Function Generator category (PHILIPS PM 5127 0.01Hz – 1MHz) giving a triangle pulses.

From ac checking, many values can be determined:

i. Resistance Ratio Measurement (R_{ratio}): These measurements can be accomplished by the sketching between (I-V) for the structure under the check (SUC), where channel 1 (ch1) correspond to the voltage through SUC and channel 2 (ch2) correspond to the current through SUC by dividing the voltage through SUC on R=100 Ω. So, figure 9 represents the ac measurements at state TE_L.

Figures should be numbered as follows: Figure1, Figure 2, … etc. Tables should be numbered as follows: Table 1, Table 2… etc.

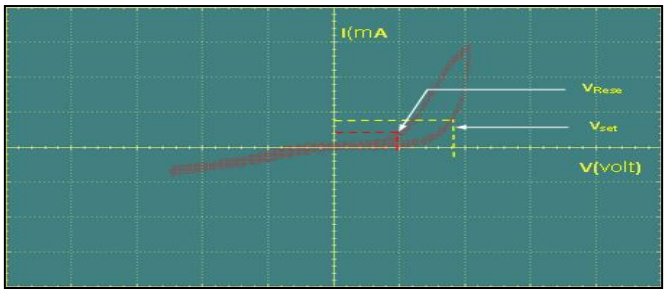

Figure 9. The ac measurements of the structure at state TE_L (these measurements were taken by using storage digital oscilloscope category (OWON MSO 7102T)).

$$R_{HRS} = {3.95\,V}/{0.138\,mA} = 28.623 \quad K\Omega \tag{1}$$

$$R_{LRS} = {1.95\,V}/{13\,mA} = 0.15 \quad K\Omega \tag{2}$$

$$R_{ratio} = R_{HRS} / R_{LRS} = 190.82 \quad (3)$$

One can be noted that the quantities of the variables RLRS, RHRS, R_{ratio}, V_{Reset} and V_{set} in ac measurements are almost equivalent to dc measurements of the structure at state of TEL.

2) Time Measurement (Ts): Through ac measurements, the switching time measurement (Ts) of the structure can be computed at state of TEL. So, from figure 9 the switching time is computed as:

$$T_S = 1 / f_S = 1 / 9.1\text{KHz} = 109.89\,\mu\text{S} \quad (4)$$

3.3 Statistical Analysis

A statistical analysis was achieved to expression the distribution range of the parameters of HR, LR, V_{set}, V_{Reset} for different cases of upper electrode zone (TEL, TEm and TEs) for the current structure (Au/CdSe/polymer/Au) without exposed it to the light as possible. This analysis is achieved by computing the following values: Mean, Medium, Minimum Value, maximum value and using the statistical diagram of distribution probability percent (Cumulative Probability%) where this diagram is used to indicate the dominance of values as well as the standard deviation (SD) calculation to find out the amount of identification of this values from the medium and in an explanative manner in cases (TEL, TEm and TEs). The statistics were achieved using the Excel program for all tables and figures.

It is observed from table 3 that there are increasing in the median value of Median HR, additional increasing in the maximum value with decreasing surface zone (TE), Also, the detection of the mediator is larger, this indicates the broader spread for a median resident and more distribution as displayed in Figure 10 shows this HR is based on the surface zone of the umbilical polarization, so the relationship is reversible, other than, the value (HR) of the TEm electrode is less inclined towards the vertical direction an indication of more stability. As for LR in Figure 11 there are an intersection among values for different upper electrode zones in addition to convergence of standard deviation values and other statistical values, this shows doesn't depending on the zone of the upper electrode.

Table 3 Statistical analysis of HR and LR values in different cases of upper electrodes zone (TE_L, TE_m and TE_s) of the structure

	TEL	**TEm**	**TEs**
LR Minimum (KΩ)	0.153	0.2	0.3
LR Maximum (KΩ)	0.167	0.24	0.37
LR Mean	0.16054	0.22253	0.33085
LR Median	0.162	0.2245	0.33
LR SD	0.0035	0.01247	0.01851
HR Minimum (KΩ)	27.8571	32.8	40
HR Maximum (KΩ)	28.1	33.3	40.5
HR Mean	27.9826	33.0675	40.2433
HR Median	27.9286	33.088	40.05
HR SD	0.05817	0.10511	0.05

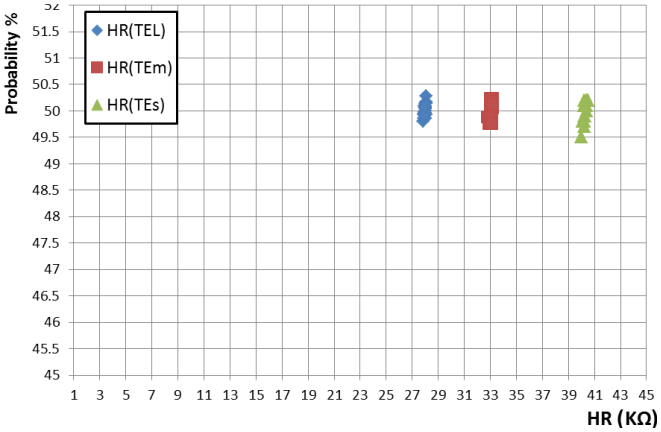

Figure 10. Percentage of the spread of HR values of the structure in different cases of upper electrodes zone (TEL, TEm and TEs).

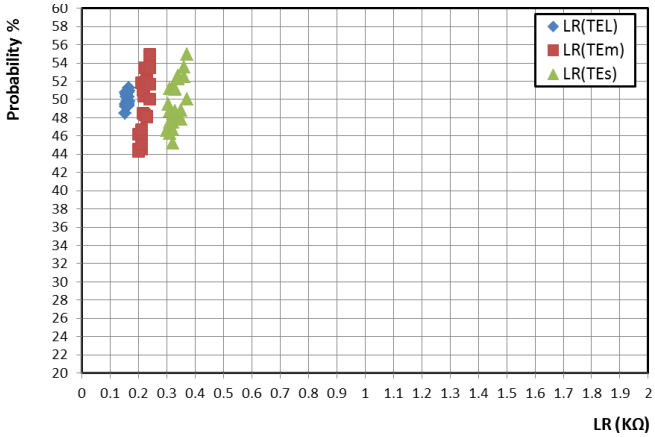

Figure 11. Percentage of the spread of LR values of the structure in different cases of upper electrodes zone (TEL, TEm and TEs).

Table 4 Statistical analysis of V_{set} and V_{Reset} Values of the structure in different cases of upper electrodes zone (TEL, TE_m and TE_s).

	TEL	**TEm**	**TEs**
V_{set} Minimum (V)	3.9	4.15	4.72
V_{set} Maximum (V)	4.1	4.3	4.85
V_{set} Mean	4.022	4.232	4.778
V_{set} Median	4.025	4.275	4.79
V_{set} SD	0.04736	0.04475	0.01
lV_{Reset}l Minimum (V)	1.9	2.15	2.71
lV_{Reset}l Maximum (V)	2.04	2.4	2.83
lV_{Reset}l Mean	1.96533	2.277	2.77433
lV_{Reset}l Median	1.945	2.3	2.755
lV_{Reset}l SD	0.03334	0.05757	0.03008

But for V_{set} and V_{Reset} as shown in table 4, there are no changing clear mentions with the convergence of maximum values, minimum values and the Median, In addition to, the value of the standard deviation indicate to the spreading within a convergent range of the structure when the upper electrodes zone are changing, this verifies that its doesn't dependent on the upper electrodes zone as shown in figures (12) and (13).

Based on the above-mentioned information, the LR, V_{Reset}, and V_{set} showed independence from the zone of the upper electrode (A) except HR is dependent on the zone of the upper electrodes.

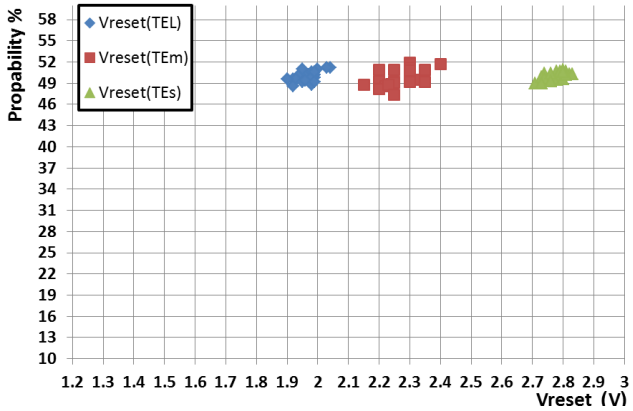

Figure 12. percentage of the spread of VReset values of the structure in different cases of upper electrodes zone (TEL, TEm and TEs).

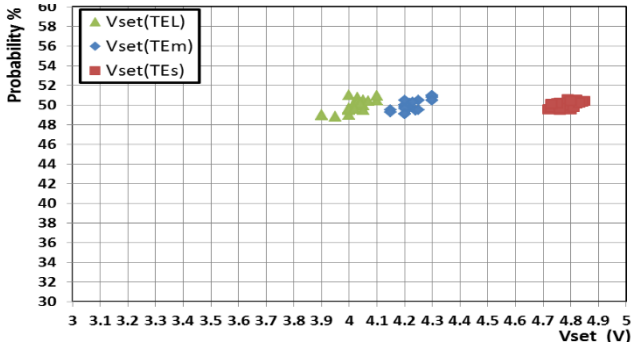

Figure 13. percentage of the spread of Vset values of the structure in different cases of upper electrodes zone (TEL, TEm and TEs).

3.4 Scanning Electron Microscope (SEM) Measurements

The SEM measurement for the structure is accomplished at the Advance Materials Research and Nanotechnology Center in University of Technology - Baghdad. See figure (14) Without embedding a thin layer of a polymer and figure (15) Shows embedding a thin layer of a polymer.

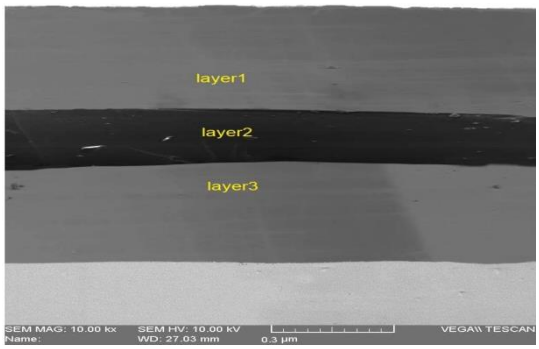

Figure 14. Cross - sectional scanning electron microscopy (SEM) images for the structure without embedding a thin layer of a polymer. [This image is taken by (SEM) underling the Advance Materials Research and Nanotechnology Center in University of Technology - Baghdad].

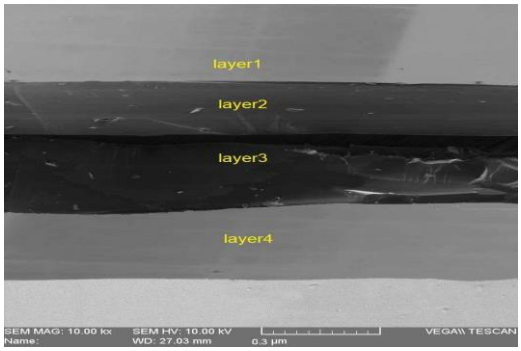

Figure 15. Cross - sectional scanning electron microscopy (SEM) images for the structure shows embedding a thin layer of a polymer. [This image is taken by (SEM) underling the Advance Materials Research and Nanotechnology Center in University of Technology - Baghdad].

The SEM image (figure 15) reveals five layers. Layers (5 and 2) represent the upper and lowest metal electrodes (Au) respectively, while layers (3 and 4) represent the cross section of two active layers (CdSe and a polymer respectively), where the layer (3) is the active martial CdSe which represents the n-type semiconductor deposited on the a lowest electrode, while the layer (4) represents a polymer (Cellulose Acetate), finally the layer (1) represents the substrate (glass)

4. CONCLUSIONS

The characteristics of a resistive switching memory structure based on embedding a Cellulose Acetate on the CdSe layer have been investigated in case of the dark. From the above analysis, it can be concluded that the resistive - switching mechanisms of RRAM structure can be noticed from the (I –V) relationships (dc and ac measurements). The structure reveals the bipolar (I–V) characteristics, because this behavior depending on the mechanism of active material (CdSe). From the investigates, the resistance in high resistive state HRS is inversely related to the zone of upper electrode TE clearly. In other words, Vset and VReset for the same structure will change inversely depending on changing the electrode zone. The polymer (Cellulose Acetate as insulator material) was embedding to the active material (CdSe as semiconductor) by Spin-coating technique so as to improve the properties of the resistive switching of the CdSe. Spin-coating technique finds itself useful in a variety of fields for thin film deposition because of its relatively low cost, high throughput and film thickness repeatability.

The LR, VReset, and Vset showed independence from the zone of the upper electrode (A) and the adoption of HR on the zone of the upper electrodes. Lastly; the resistance ratio (Rratio) is directly proportional with the (A). The examining structure has several characteristics, such as Vset= 3.9Volt, VReset = -1.9Volt and Rratio about 176 in case of TEL. Generally, the above values (Vset and VReset) represent a high values in corresponding to the other structures, but Rratio represent accepted values for resistive switching of the current structure, So, as suggestion in future work, the changing of the a polymer (Cellulose Acetate) with another good polymer such as (Cellulose Nitrate) may enhance the properties of the present structure and studding the current structure in case of light intensity varying on it.

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REFERENCES

[1] Chen, C., Yang, Y., Zeng, F., & Pan, F. Bipolar resistive switching in Cu/AlN/Pt nonvolatile memory device. Applied Physics Letters, **97**, 8 (2010) 083502.

[2] Bez, R., Camerlenghi, E., Modelli, A., & Visconti, A. Introduction to flash memory. Proceedings of the IEEE **91**, 4 (2003) 489-502.

[3] Li, Y., Long, S., Liu, Q., Lü, H., Liu, S., & Liu, M. An overview of resistive random access memory devices. Chinese Science Bulletin **56**, 28-29 (2011) 3072.

[4] Tu, C.-H. (2008). Electrical switching and memory behaviors in organic-based devices.

[5] Kissinger, N. S., Jayachandran, M., Perumal, K., & Raja, C. S. Structural and optical properties of electron beam evaporated CdSe thin films. Bulletin of Materials Science **30**, 6 (2007) 547-551.

[6] Kaur, R., & Tripathi, S. Study of conductivity switching mechanism of CdSe/PVP nanocomposite for memory device application. Microelectronic Engineering **133** (2015) 59-65.

[7] Wu, D., Xu, T., Shi, Z., Tian, Y., Li, X., Yu, Y., & Jiang, Y. Two-terminal nonvolatile resistive switching memory devices based on n-CdSe NR/p-Si heterojunctions. Journal of Alloys and Compounds **695** (2017) 1653-1657.

[8] Hu, D., Zhang, G., Yang, H., Zhang, J., Chen, C., Lan, S., . . . Guo, T. High-performance nonvolatile organic transistor memory using quantum dots-based floating gate. IEEE Transactions on Electron Devices **64**, 9 (2017) 3816-3821.

[9] B. K. Kaushik. Nanoelectronics: Devices, Circuits and Systems (Micro and Nano Technologies) 1st Edition. Elsevier **476** (2018).

[10] Kim, N.-R., Kim, S.-W., Bae, J.-H., & Kang, S.-W. Multi-level resistive write-once-read-many memory device based on CdSe/ZnS quantum dots and ZnO nanoparticles. Thin Solid Films, (2020) 138120.

[11] Pena, D. J., Mbindyo, J. K., Carado, A. J., Mallouk, T. E., Keating, C. D., Razavi, B., & Mayer, T. S. Template growth of photoconductive metal− CdSe− metal nanowires. The Journal of Physical Chemistry B 106, 30 (2002) 7458-7462.

[12] Padiyan, D. P., Marikani, A., & Murali, K. Influence of thickness and substrate temperature on electrical and photoelectrical properties of vacuum-deposited CdSe thin films. Materials Chemistry and Physics **78**, 1 (2003) 51-58.

[13] Wu, D., Jiang, Y., Yu, Y., Zhang, Y., Li, G., Zhu, Z., . . . Jie, J. Nonvolatile multibit Schottky memory based on single n-type Ga doped CdSe nanowires. Nanotechnology **23**, 48 (2012) 485203.

[14] Seo, S., Lee, M., Kim, D., Ahn, S., Park, B.-H., Kim, Y., . . . Kim, S. Electrode dependence of resistance switching in polycrystalline NiO films. Applied Physics Letters **87**, 26 (2005) 263507.

[15] Fischer, S., Thümmler, K., Volkert, B., Hettrich, K., Schmidt, I., & Fischer, K. Properties and applications of cellulose acetate. Paper presented at the Macromolecular symposia, (2008).

[16] Li, Y., Long, S., Liu, Q., Lü, H., Liu, S., & Liu, M. An overview of resistive random access memory devices. Chinese Science Bulletin **56**, 28-29 (2011) 3072.