International Journal of Nanoelectronics and Materials
Volume 12, No. 1, Jan 2019 [105-122]

The Effect of Dielectric Surface Modification and Heat-treatment on the Performance of Rubrene based Organic Field-effect Transistor

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Received 12 March 2018; Revised 3 July 2018; Accepted 10 August 2018

ABSTRACT

In this work, bottom gate top contact structured organic field-effect transistors (OFETs) were fabricated using Rubrene as active material and SiO_2 as the dielectric on n-type silicon wafer by thermal evaporation method. The effect of dielectric surface modification and abrupt heat treatment on the crystallinity of Rubrene thin film and its influence on the performance of OFETs were investigated. The surface morphologies and the crystal structure of Rubrene films were characterized using differential scanning calorimetry, X-ray diffraction (XRD) and atomic force microscopy. It is observed that the dielectric surface affects the crystalline structure of Rubrene thin film as well as the electrical performance of the OFETs. Thermal transition of Rubrene from amorphous state to highly crystalline state was observed after abrupt heat treatment. It is observed that highly crystalline Rubrene thin films can be obtained by carefully deploying the rapid heat treatment method followed by surface treatment. The electrical properties of the OFETs such as field effect mobility, threshold voltage and current on/off ratio are evaluated using the V-I characteristics and the results are compared with the published data. Improvements in the performance of OFET are evident due to the improved crystallization and highly ordered structure of Rubrene molecules.

Keywords: Rubrene, Organic Field Effect Transistor, Dielectric Surface Modification, Rapid Heat Treatment, Crystallinity, Field Effect Mobility.

1. INTRODUCTION

In recent years, applications of organic film electronic devices are emerging as viable options for low-cost, flexible electronic applications. Organic field effect transistors (OFETs) have received considerable attention for applications in the driving elements of active matrix flat panel displays, large-area sensor arrays and radio-frequency identification tags [1]. Among the materials, Rubrene has drawn considerable research interests due to its high carrier mobility of 20 cm^2/Vs in its single crystal form [2]. Many studies on Rubrene single crystals have been carried out [3] and the performance of Rubrene single crystal based OFETs have been well demonstrated [4]. For practical applications, however, Rubrene based OFETs have achieved only limited success because of difficulties in obtaining a Rubrene thin film of high crystalline quality by conventional thermal evaporation methods. This is attributed to the non-planar molecular Rubrene structure consisting of a tetracene backbone and four phenyl side groups.

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The deposition of Rubrene molecules on solid substrates, such as SiO_2, results in thin films with poor crystalline order. OFETs based on such amorphous films exhibit very low field effect mobility of 10^{-4} cm^2/Vs [5]. Several efforts have been made for producing crystalline Rubrene thin films over dielectric layers for large area electronics, including "hot-wall" deposition techniques [6], in-situ vacuum annealing [5], solution-processing techniques [7] and organic inducing layer [8]. Although these techniques have been successfully used in the fabrication of OFETs, they suffer from either rigorous experimental validation and/or possess lower charge carrier mobility which is in the range of 0.002-0.7 cm^2/Vs. The mobility achieved is still lower than 1 cm^2/Vs, which is the critical value for technical applications [9]. However, Lee and co-workers [10] have reported an abrupt heating technique to fabricate crystalline Rubrene thin films. This approach according to the authors has resulted in an average mobility of 1.21 cm^2/Vs.

A review from recently published research observed that the charge carrier transport in OFET is strongly affected by the first few semiconductor monolayers next to the semiconductor-insulator interface [11]. Therefore, the physical state of the dielectric surface that affects morphology of the initial layer of the semiconducting active layers near the interface is very important to enhance the performance of OFETs. Among the interfacial factors, insulator surface roughness, surface energy, surface polarity and dielectric constant of dielectrics are considered as important parameters that affect the performance of the OFET. Recently, a lot of efforts have been focusing on optimization of the conditions of the surface of the dielectrics using various treatment techniques [12]. It is well established that by chemical treatment of the gate dielectric surfaces with Octadecyltrichlorsilane (OTS), the self-assembled monolayers (SAM) significantly reduce the trap states and change the surface energy. This facilitates the formation of an orderly structure in the organic films grown on the top, especially the first monolayer which is very critical to improve the interface between the organic semiconductor and the dielectric [13].

In this investigation, modifications in rapid heat treatment of Rubrene thin films has been investigated and the benefits of surface modification of SiO_2 with OTS in improving the performance of OFETs have been analyzed.

2. EXPERIMENTAL DETAILS

2.1 Materials

The main elements of an OFET are the three contacts (source, drain and gate), an active semiconductor material and a dielectric layer. The selection of the OFET architecture has a significant effect on the electrical characteristics of the device due to the differences in charge injection. However, OFET is often limited by the restrictions in processing methods or the incompatibility of the materials used in the fabrication. Thus, important factors in tuning the device performance are the choice of materials and their optimization.

In the present work, top contact bottom gate transistor architecture was used in the fabrication, deploying doped silicon wafer of superior quality with a resistivity of 1-10 ohm-cm as the substrate, thermally grown SiO_2 as the dielectric, and Rubrene as the organic semiconductor with gold (Au) as electrodes. Octadecyltrichlorsilane (OTS) is a self-assembled monolayer in toluene solvent was used for the modification of the surface of SiO_2. Isopropyl alcohol, acetone, ethanol and de-ionized water were used as substrate cleaning and etching agents. Shadow masks were used for the deposition of source and drain electrodes. The details of the materials used in this work are shown in Table 1.

2.2 Sample Preparation

Initially, wafers were cleaned to remove the metallic and organic impurities by using procedures RCA1 and RCA2 as outlined in literature [14]. A 200 nm thick SiO_2 oxide layer was grown over the clean wafers by dry oxidation method. Etching of the backside oxide formed during oxidation was carried out in buffered HF solution (BHF) before metallization. After back oxide etching, Au gate electrode was deposited at the back surface of wafers by thermal evaporation. Then, the SiO_2/Si substrate was immersed in a 0.1 Wt. % solution of OTS in toluene for 12 h in a glove box to form the OTS-SAM on the SiO_2/Si substrate. Rubrene thin film of thickness 80 nm was deposited by thermal evaporation technique at a rate of 1.8 $\dot{A}$/s both onto the bare SiO_2 substrate and the OTS-treated SiO_2 substrate at 50°C under a vacuum of 1.2×10^{-6} mbar individually. Subsequently, the Rubrene thin film on SiO_2 substrate was subjected to different heat treatments in a nitrogen filled glove box in order to understand the effects of heat treatment on the crystallinity of Rubrene thin film. Top-contact OFETs with Rubrene as the active layers were fabricated for evaluating the V-I characteristics. To form drain and source electrodes, Au contacts were thermally evaporated through a shadow masks. The mask was patterned with a fixed channel length (L) of 30 μm and width (W) of 3000 μm respectively. The details of the samples fabricated are shown in Table 2.

Table 1 Details of materials used for the fabrication of OFET

Sl. No.	Material	Properties/Grade	Source
1	Si-wafer	N-Si <100> wafers	Topfil, Brazil
2	Rubrene	≥ 98 % purity	Sigma Aldrich, USA
3	Gold	Grade: 59 karat	Bling corolla, UK
4	Shadow masks	Stainless steel Kapton	Laser Micromachining Ltd, UK
5	Isopropyl alcohol	Natural, ≥98 % purity	Sigma Aldrich, USA
6	Acetone	Density: 0.791 g/mL	Sigma Aldrich, USA
7	Ethanol	~ 96 % purity	Sigma Aldrich, USA
8	Toluene	~ 99.8 % purity	Sigma Aldrich, USA
9	OTS	≥ 90 % purity	Sigma Aldrich, USA

Table 2 Identification of the samples fabricated

Sample identification	Description
S1	Rubrene on SiO_2/Si substrate heat-treated at 125 ℃ for 30 min.
S2	Rubrene on SiO_2/Si substrate heat-treated at 150 ℃ for 5 min.
S3	Rubrene on SiO_2/Si substrate heat-treated at 175 ℃ for 1 min.
S3(OTS)	Rubrene on OTS-coated SiO_2/Si substrate heat-treated at 175 ℃ for 1 min.

3. MEASUREMENT METHODS

The following measurements were carried out in order to study the role of different parameters in the performance of OFETs.

3.1 Thickness

Spectroscopic Ellipsometer model M-2000 of M/s J.A. Woolam was used to measure the thickness of the SiO_2 layer based on the changes in polarization when light is reflected or transmitted from the material structure. Dektak XT Surface Profilometer from M/s Bruker was used to measure the thickness of Rubrene thin film based on the film step height measurement method.

3.2 Differential Scanning Calorimeter

The Differential Scanning Calorimeter (DSC) data was used for monitoring the transition temperature and exothermic reactions including those involved in the base material. DSC model Q200 of M/s TA instrument was used for measurement of thermal transition of Rubrene thin film from amorphous to crystalline state at a heating rate of 80°C/min.

3.3 X-ray Diffraction (XRD)

X-ray diffraction analysis was carried out using Rigaku miniflex-II desktop system with high intensity Cu Kαl irradiation (λ=1.5406 Å) at a scan speed of 5 °/min.

3.4 Atomic Force Microscopy

The surface morphology of the Rubrene thin film was characterized and the top-view of Rubrene based OFET with the source and drain (Au) was captured using atomic force microscope (AFM) of M/s Bruker Dimension ICON in the tapping mode.

3.5 V-I Characteristics

The electrical characteristics of the Rubrene OFETs were determined using the Agilent B1500A device analyzer. The drain-source and gate-source voltages were swept from 0 to -50 V and the corresponding drain-source current was measured.

4. RESULTS AND DISCUSSION

4.1 Thermal Properties of Heat Treated Rubrene Thin Films

For understanding the resulting crystalline structures which evolves during heat treatment, and to analyze the thermal transition of the amorphous Rubrene the DSC thermogram of samples S1, S2 and S3 were used and are shown in Figure 1. As seen from the thermograms, two different crystallization exotherms at 110-150℃ and 150-175℃ were observed in case of S2 and S3 samples and there is no crystallization exotherm in case of S1. This result shows that crystalline structures begin to form at 110°C and the degree of crystallinity increases with the increase in temperature. During heat treatment, it is observed that on rapid heating of Rubrene thin film at a relatively lower temperature, there are no crystallite formation in the film. Interestingly, when the temperature was increased to 150℃, formation of Rubrene crystalline structure was observed. With further increase of temperature to 175℃, there is improvement in Rubrene crystalline structure. This conclusively proves that the crystallization behavior of Rubrene thin film is strongly dependent on the temperature.

Time-temperature-transformation diagram of Rubrene thin films when subjected to the two heating rates are shown in Figure 2. It is observed that the formation of undesired discontinuous crystallites takes place when the heating rate is low. This may be due to the slow increase in film temperature leading to longer time for the crystallization to occur in the organic Rubrene structures. This is prevented by using a higher temperature at sufficiently increased heating rates. It is observed that the desirable heating temperature and rate for Rubrene is 175℃ for 1 minute [15]. These findings are in line with the reported findings in literature that at a particular temperature, under certain time period, the crystallization of the Rubrene thin films displays disk-like crystalline domains whose nucleation and growth follow known phase transformation kinetic. From literature, it is also observed that during the heat treatment, the film undergoes transition from the predominantly polycrystalline triclinic crystal structure to single crystal orthorhombic structure followed by the polycrystalline growth of the orthorhombic polymorph [16].

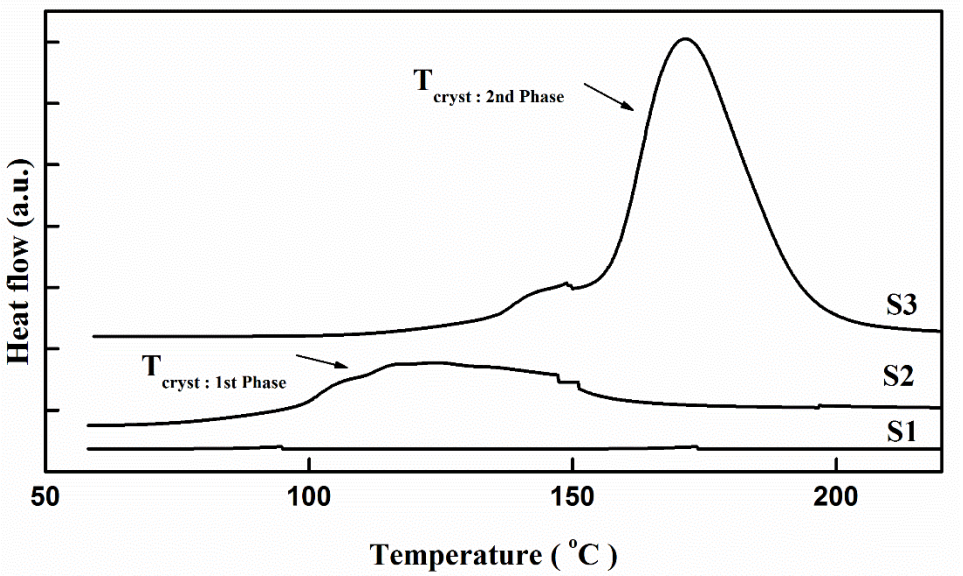


Figure 1. DSC thermogram of samples S1, S2 and S3.

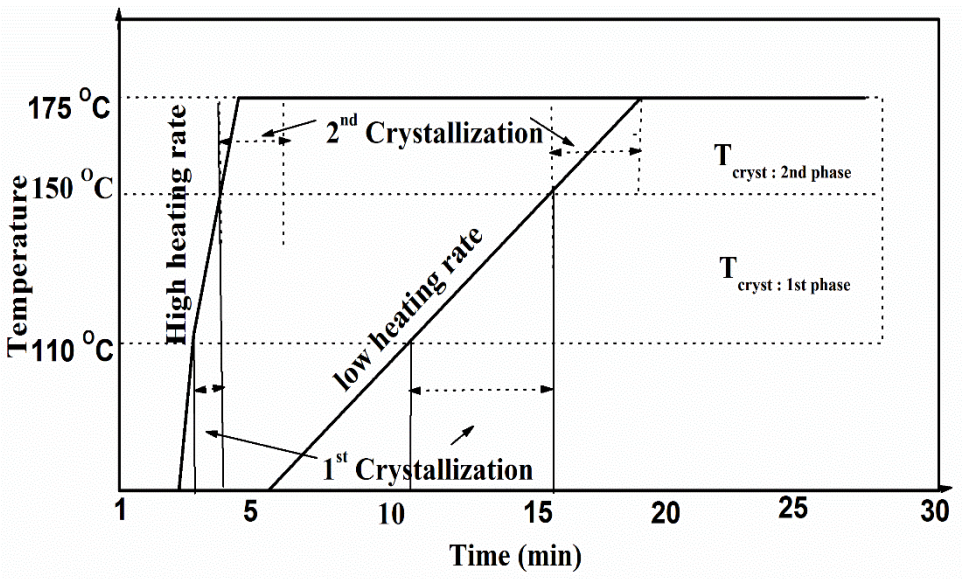


Figure 2. Time-temperature-transformation diagram of Rubrene.

4.2 Crystal Structure Analysis of Heat Treated Rubrene Thin Films

To identify the crystalline nature of the heat treated Rubrene thin films, X-ray diffraction (XRD) and atomic force microscopy analysis were carried out.

4.2.1 Analysis Using X-Ray Diffraction

The XRD spectra of the samples S1, S2 and S3 are shown in Figure 3. It is observed that the XRD peak intensity of the sample S2 is higher than that of sample S1, whereas multiple peaks with lower intensity are observed in the case of sample S3. This result shows that the XRD peak intensity increases when increasing temperature. Higher XRD peak intensity indicates the presence of large crystalline fraction. The XRD data of the heat treated Rubrene thin films are shown in Table 3. The samples S1 and S2 have one small peak at 6.58° (d-spacing of 13.47 Å) and at 6.55° (d-spacing of 13.50 Å) respectively corresponding to 200 plane of Rubrene crystal, while the sample S3 has two small peaks at 6.63° (d-spacing of 13.43Å) and 13.25° (d-spacing of 6.73Å) respectively corresponding to 200 and 400 planes of Rubrene crystal. Full width at half maximum (FWHM) values of XRD peaks differ with the variation of peak intensity for different temperatures. The smaller FWHM value, lesser d-spacing, and higher peak intensity (2θ) of sample S3 indicates that it has the larger crystal grain size as compared to samples S1 and S2 [17, 18]. The larger grain size signifies a good interconnectivity of grains. The XRD results point out that the Rubrene thin films S1 and S2 which are heated at lower temperature for longer durations have smaller grain size while the Rubrene thin film S3 which is heated at higher temperature for shorter duration has larger crystal grain size. This is due to the greater diffusion of Rubrene molecules at higher temperatures resulting in the formation of larger grains [10].

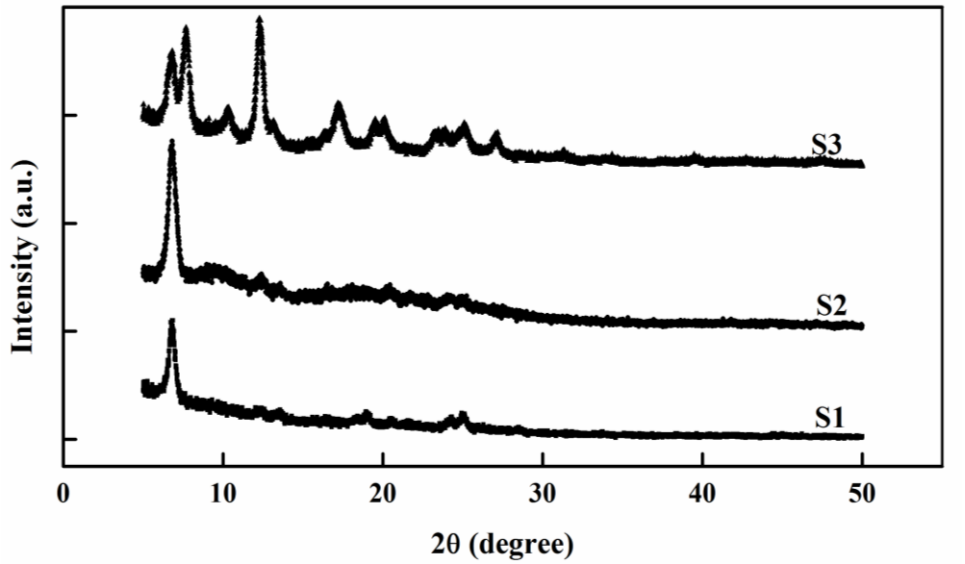


Figure 3. X-Ray Diffraction spectra of samples S1, S2 and S3.

Table 3 XRD data of Rubrene thin films

Sample identification	2θ° (± 0.10)	d-spacing (Å) (± 0.05)	FWHM (± 0.1)
S1	6.58	13.47	0.41
S2	6.55	13.50	0.39
S3	6.63, 13.25	13.43, 6.73	0.34, 0.32

4.2.2 Surface Morphologies of Rubrene thin films

The surface morphology of Rubrene thin films deposited on SiO_2 heated at different temperatures and duration analyzed using AFM is shown in Figure 4. The AFM images clearly show that the grain size and grain boundaries of Rubrene thin films are different. Sample S1 contains few micro-grains of small size of 20-50 nm with more grain boundaries and average roughness of 11.53 nm. Interestingly, the average grain size of sample S2 and S3 are observed to be 100-300 nm and 1000-1500 nm respectively with reduced grain boundaries. The measured surface roughness of sample S2 is 8.38 nm (rms) and it is higher than the roughness of sample S3 which is 5.56 nm. This is due to the fact that insufficient heating time duration induces only partial coverage of the crystalline film over SiO_2 surface, whereas a higher heating duration results in pores within the crystalline film.

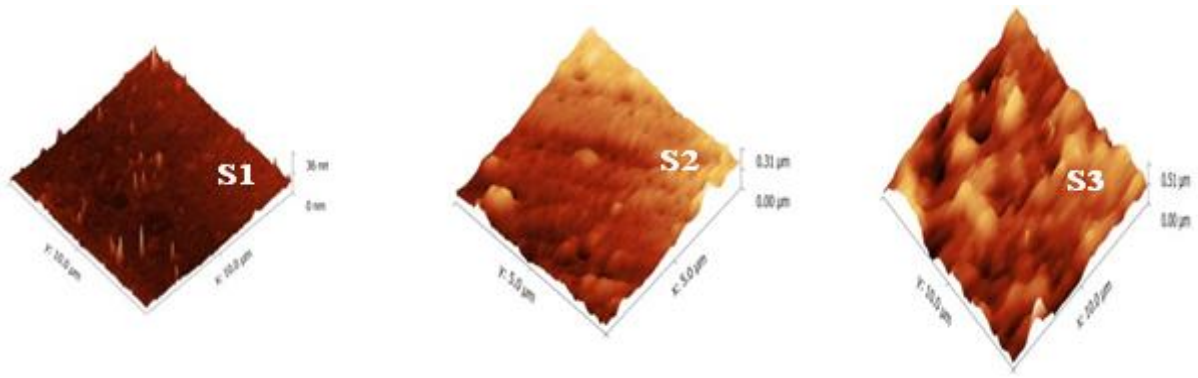


Figure 4. Atomic force microscope images of surface of samples S1, S2 and S3.

4.2.3 Study of Rubrene Crystalline Film on OTS Treated Sio₂ Dielectric Surface

The crystallinity and morphology of Rubrene thin films at the top of OTS-SAM-treated SiO_2 were investigated using XRD and AFM techniques. The XRD spectra of Rubrene thin film fabricated using the OTS treated SiO_2 surface by abrupt heating is shown in Figure 5. It is observed that the XRD peak intensity is significantly different after surface modification and heat treatment. The FWHM value, d-spacing and peak intensity of sample S3 (OTS) shown in Table 4 and the results confirm improvements in the crystallinity of Rubrene after surface treatment.

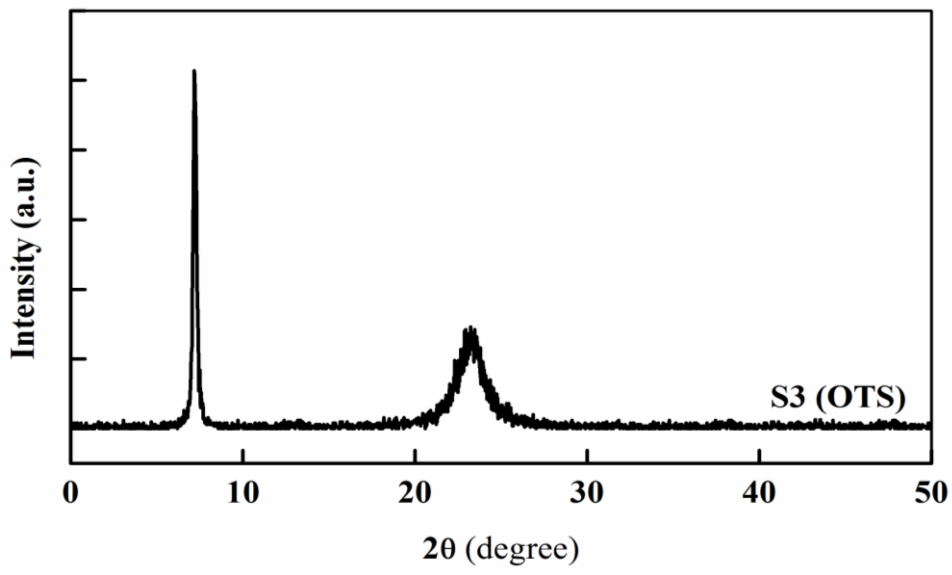


Figure 5. X-Ray Diffraction pattern of sample S3 (OTS).

Table 4 XRD data of Rubrene thin film sample S3 (OTS)

Sample identification	2θ°(± 0.10)	d-spacing (Å) (± 0.05)	FWHM (± 0.1)
S3 (OTS)	7.24	13.38, 3.82	0.17, 0.52

The top view of AFM image of the top contact OFET (Sample S3 (OTS)) with heat treated Rubrene as active layer on OTS-SAM treated SiO_2 dielectric surface is shown in Figure 6. The Rubrene thin film with the modified dielectric surface appears nearly flat. The surface roughness is 2.8 nm (average) because of the reduced surface roughness, the electrodes adhere well to the polymer and this can be observed in Figure 6. The lower values of surface roughness signify larger grain growth on the surface. This fact helps in the enhancement of the void-less grain formation between the inter-grains of the first surface monolayer. This is due the change of SiO_2 surface property from hydrophilic to hydrophobic nature with reduced surface energy [19].

Thus, it is very evident that the treatment of OTS-SAM on SiO_2 has an important role to play in improving the crystallinity of the Rubrene thin films. It is stated by H. M. Lee and co-workers [10] that surface treatment would not be required if heat treatment is optimized. This study has proven that surface treatment can further improve the crystallinity of the fabricated thin films. The increase in grain size and the reduction in roughness in case of heat treated Rubrene surface on SiO_2 is well corroborated by the results of XRD analysis

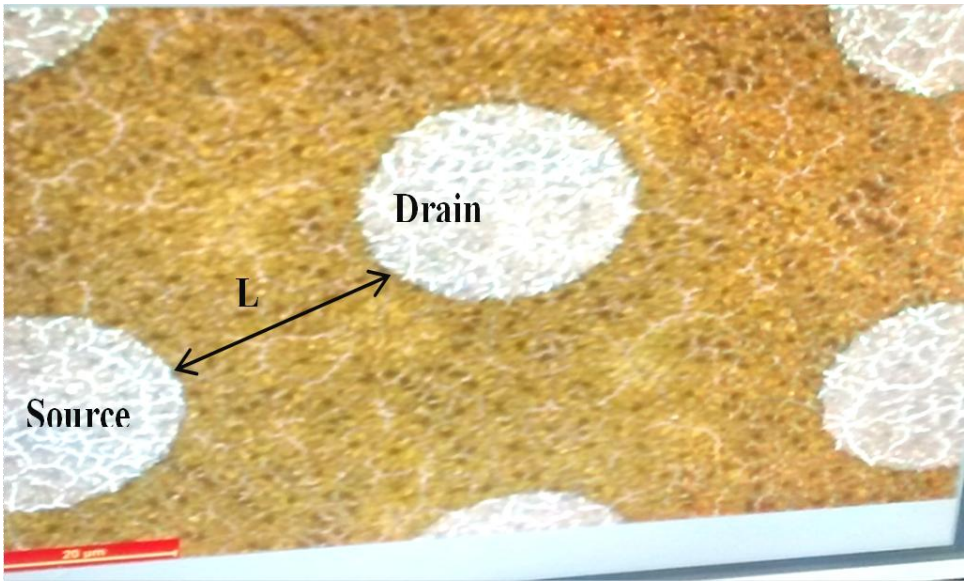


Figure 6. Top view of the OFET sample S3 (OTS).

4.3 Electrical Characteristics of the Ofets with Heat-Treated Rubrene Thin Films

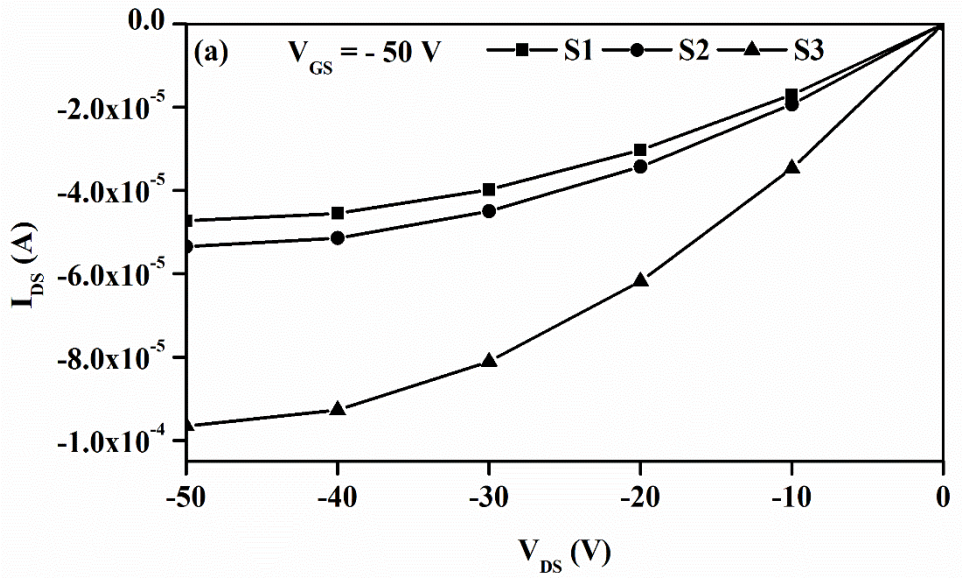
4.3.1 V-I Characteristics

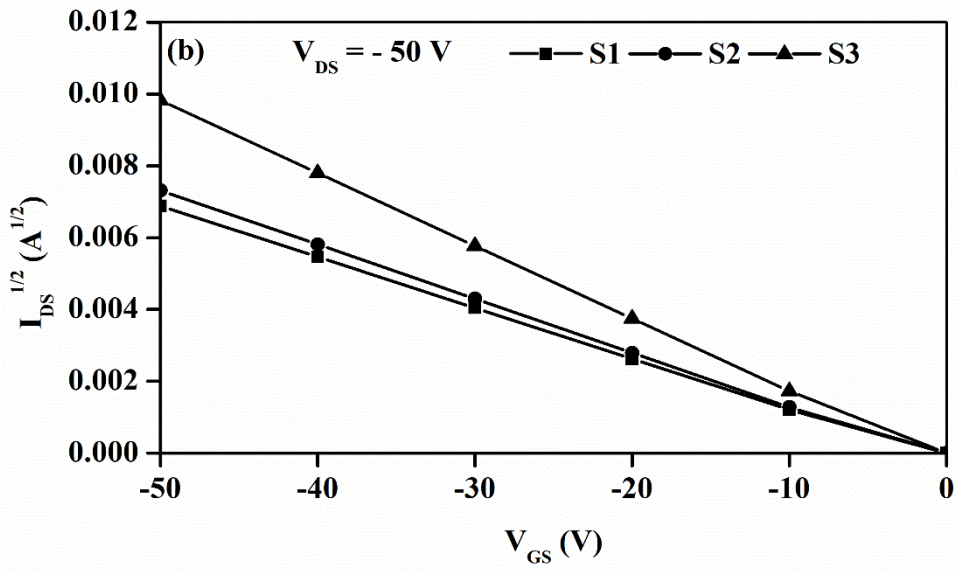
To confirm the effectiveness of the rapid heating method, the V-I characteristics of the OFETs are established. The output characteristic (I_{DS} vs. V_{DS}) at a gate-source voltage (V_{GS}) of -50 V and the drain-source voltage (V_{DS}) of 0 to -50 V were determined and are shown in Figure 7(a). The typical transfer characteristics ($\sqrt{I_{DS}}$ vs. V_{GS} and Log (I_{DS}) vs. V_{GS}) were determined at V_{DS} of -50 V and V_{GS} of 0 to -50 V in steps of -10 V as shown in Figure 7(b) and 7(c).

It is observed that the devices exhibit typical p-type transistor characteristics. The V-I characteristics of the sample without heat treatment are not shown because the generated currents were too low. The field effect mobility (μ) of the OFET is estimated from the slope of the plot of square root of (I_{DS}) vs. V_{GS} and by using the following equation in the saturation region:

$$I_{DS,\,sat} = (WC_i / 2L)\, \mu_{sat}\, (V_{GS} - V_T)^2 \quad (1)$$

In Eq. (1), W and L are the channel width and length respectively, C_i= 17.3 nF/cm^2 is the capacitance per unit area of the SiO_2 layer of the OFET, V_{GS} is the gate voltage and V_T is the threshold voltage. The x-intercept is extrapolated to arrive at the value of the threshold voltage. The computed values of the device parameters were summarized in Table 5.





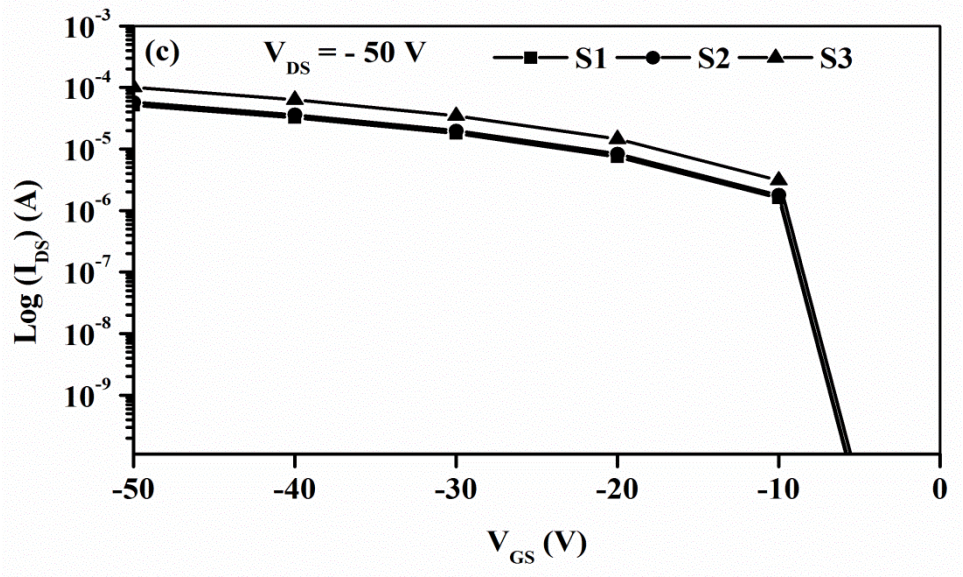


Figure 7. V-I characteristics of OFET for samples S1, S2 and S3 (a) Output characteristic: I_{DS} vs. V_{DS} (b) Transfer Characteristic: $\sqrt{I_{DS}}$ vs. V_{GS} and (c) Transfer characteristic: Log (I_{DS}) vs. V_{GS}.

Table 5 Summary of performance parameters of Rubrene OFET

OFET Sample identification	Performance parameters					
	I_{DS} (μA)	V_{GS} (V)	μ (cm^2/Vs)	V_T (V)	I_{on}/I_{off}	S (V/dec)
S1	47.5	50	0.025	- 4	10^5	0.93
S2	53	50	0.028	- 3	10^5	0.85
S3	96	50	0.049	- 2.5	10^6	0.67

It is observed from Table 5 that the heat treatment is very effective in improving the device parameters. The devices (S1 to S3) show significant improvement when the heating temperature was increased from 125°C to 175°C. This indicates that the changes in the substrate temperature lead to different morphologies and grain size. The organization of Rubrene molecules is better in case of S3 and thus better electrical performance of the OFET device is observed. The preferred heating temperature (175°C) and rate (1 minute) of this study are observed to yield higher field effect mobility (μ) and on/off current ratio (I_{on}/I_{off}) and it also contributes towards the decrease in the values of threshold voltage (V_T) and subthreshold swing (S). The improved mobility of the sample S3 is consistent with the grain size and XRD intensity.

4.3.2 V-I Characteristics of Rubrene Crystalline Film Ofots Treated Sio_2 Dielectric Surface

Since the mobility values were considerably low, sample S3 was subjected to surface treatment using OTS. The transfer and output characteristics of OFET devices with heat treated Rubrene as active layer on OTS-SAM treated SiO_2 dielectric surface are presented in Figure 8 (a) and 8(b). The results extracted from Figure 8(a) and 8(b) are shown in Table 6. It is observed that SiO_2, when treated with OTS prior to deposition of Rubrene, yields highest drain current (I_{DS}) of 390 μA at the lower gate bias of -20 V. Further, the device exhibits higher field effect mobility of 1.36 cm^2/Vs and on/off current ratio of 10^7 under ambient conditions. It is noteworthy to mention that the field effect mobility achieved is much higher than those of Rubrene crystalline films grown on bare SiO_2. This indicates that the surface modification of SiO_2 increases the accumulation of charge at the OSC/insulator interface by reducesing the trap states

substantially and this in turn improves the performance of the device [13,19]. These results suggest that the surface modification of SiO_2 with OTS is very effective and a promising method for polycrystalline Rubrene channel formation which involves transition from amorphous to crystalline phase during heat-treatment.

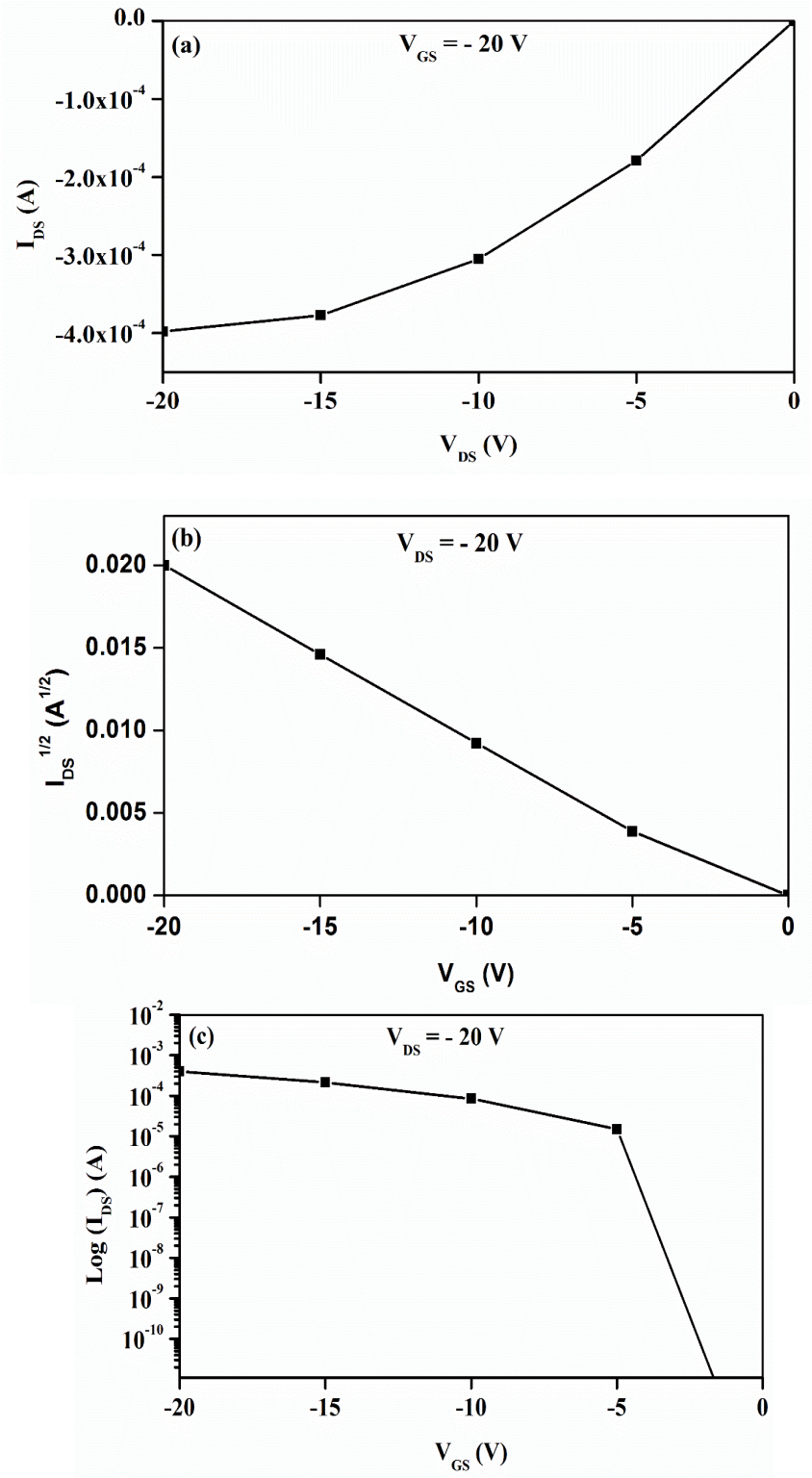


Figure 8. I-V characteristics of OFET for sample S3 (OTS) (a) Output characteristic: I_{DS} vs. V_{DS} (b) Transfer characteristic: $\sqrt{I_{DS}}$ vs. V_{GS}(c) Transfer characteristic: Log (I_{DS}) vs. V_{GS}.

Table 6 Summary of performance parameters of Rubrene OFET sample S3 (OTS)

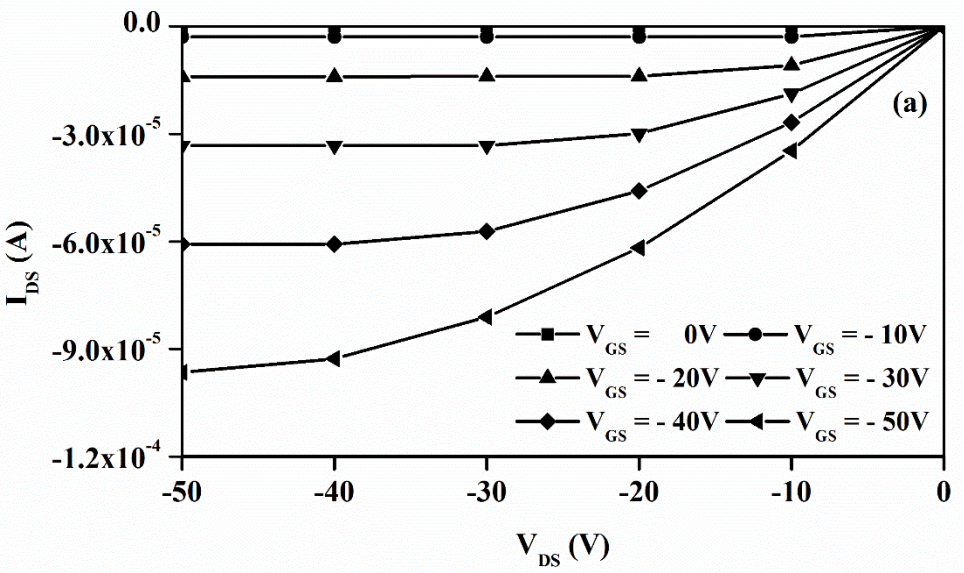
Sample identification	Performance parameters					
	I_{DS} (μA)	V_{GS} (V)	μ (cm^2/Vs)	V_T (V)	I_{on}/I_{off}	S (V/dec)
S3 (OTS)	390	20	1.36	- 0.8	10^7	0.59

4.3.3 Dependence of Mobility on the Gate Voltage

To study the gate bias dependency of the field effect mobility, the output characteristics of the device was determined for the samples S3 and S3 (with OTS treatment) at different gate source voltages and the results are presented in Figure 9 (a) and 9(b) respectively.

It is observed that the drain current increases quasi-linearly with gate voltage. The Rubrene OFET shows typical p-type semiconductor characteristics and the carrier transport is due to charge accumulation at the organic-metal interface. A negative gate voltage induces a uniform positive charge density at the SiO_2-Rubrene channel. Further, the accumulated charge and its distribution are dependent on the gate bias (V_{GS}) and the drain-source voltage (V_{DS}). The increase in drain current depends on the mobility of charge carrier which in turn is a function of the gate bias voltage of the Rubrene device.

Thus, the gate voltage dependence of the mobility is a function of the quantity of charge released, which in turn depends on the Fermi level at the insulator semiconductor interface. The mobility range for the sample S3 is estimated to be 0.0098-0.049 cm^2/Vs for variation in V_{GS} from -10 to -50 V, whereas it ranges from 0.34-1.36 cm^2/Vs for the sample S3 (OTS treated) for the variation in V_{GS} from -5 to -20 V. These results indicate that the value of mobility is depend on the gate voltage [20, 21]



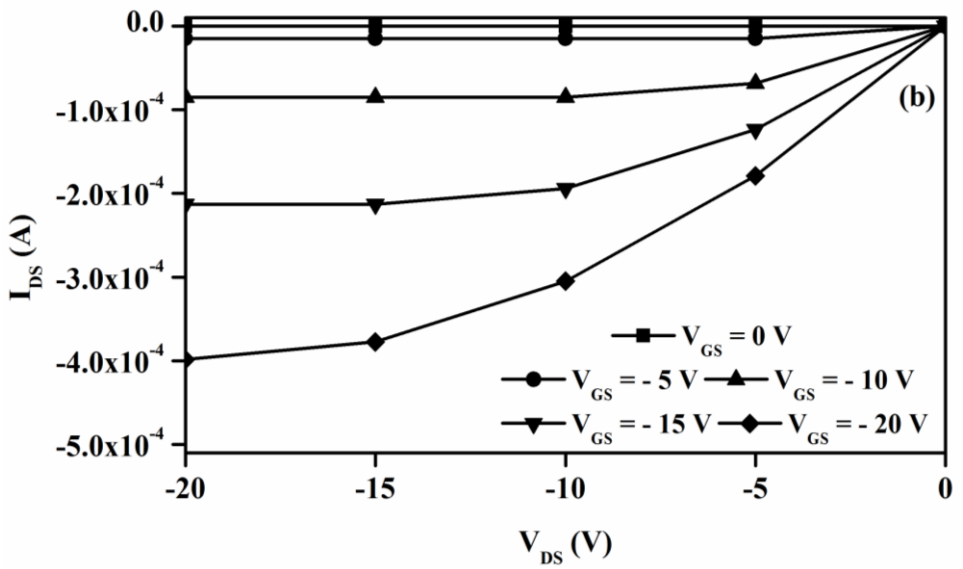
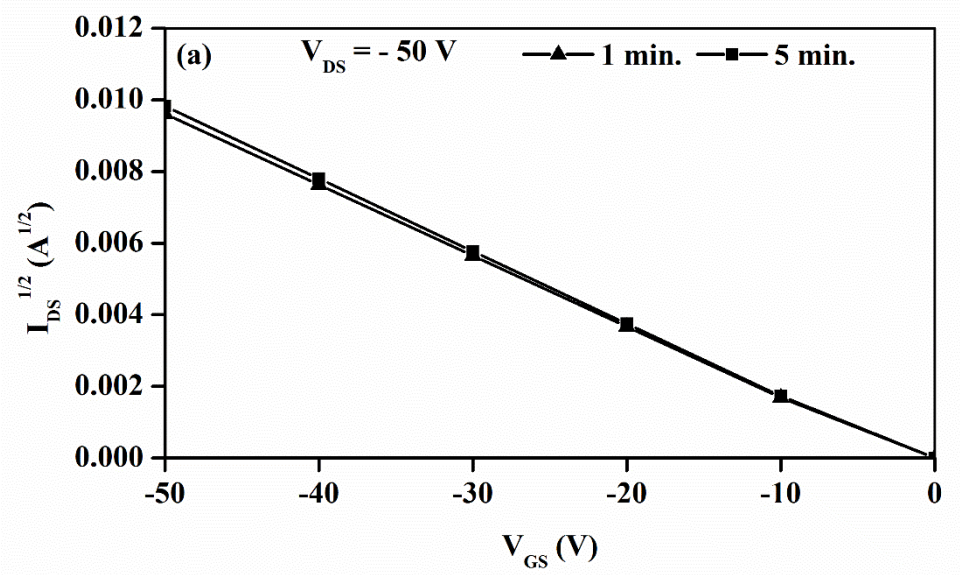


Figure 9. Variations in drain current (I_{DS}) with drain voltage (V_{DS}) for different gate voltages (V_{GS}): (a) sample S3 (b) sample S3 (OTS treated).

4.3.4 Dependence of Sweep Rate on the Performance of OFET and the Bias-Stress Effect

In order to investigate the dependence of the sweep rate on the performance of OFET, the transfer characteristics of Rubrene OFET were determined at two different sweep periods of the gate voltages of 1 and 5 minutes respectively. As shown in Figure 10(a) and 10(b), there was practically no dependence of the sweeping rate on the transfer characteristics of the OFET.



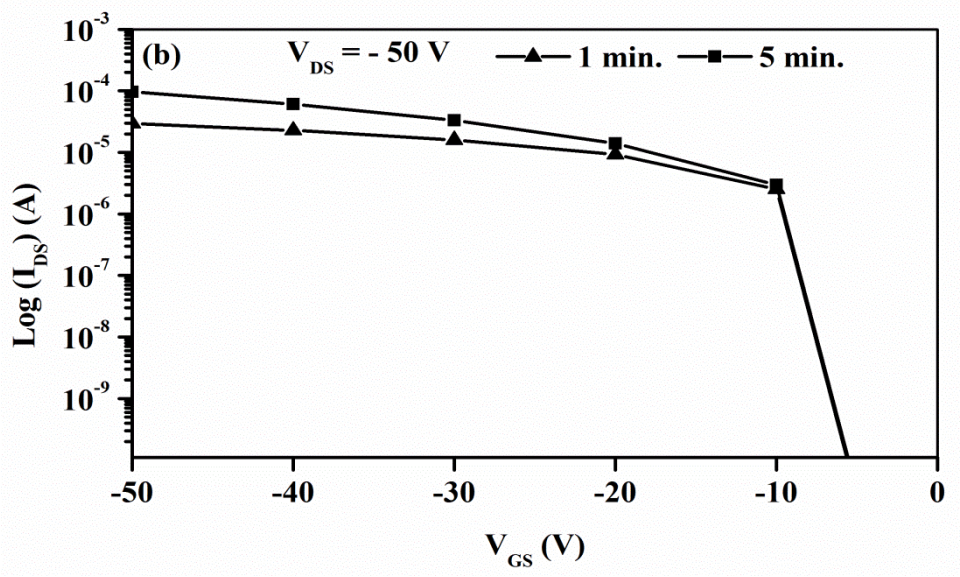


Figure 10. Transfer characteristics: (a) Log (I_{DS}) vs. V_{GS} (b)$\sqrt{I_{DS}}$vs. V_{GS} scanned in the forward and reverse direction continuously at the V_{DS} = - 50 V at different scan of 1 min. and 5 min.

The bias stress effect on operational stability of Rubrene OFET was investigated by monitoring the drain current under a continuous bias stress of V_{GS} = V_{DS} = - 50 V. As shown in Figure 11, after 1000 second of bias, the drain current of the Rubrene OFET decreased to 87% of its initial value. This is due to the formation of long term charge trapping either in the Rubrene channel or at the interface with the SiO_2 dielectric under continuous bias stress [22]. However, no gradual shift of the threshold voltage towards the applied gate bias voltage is observed.

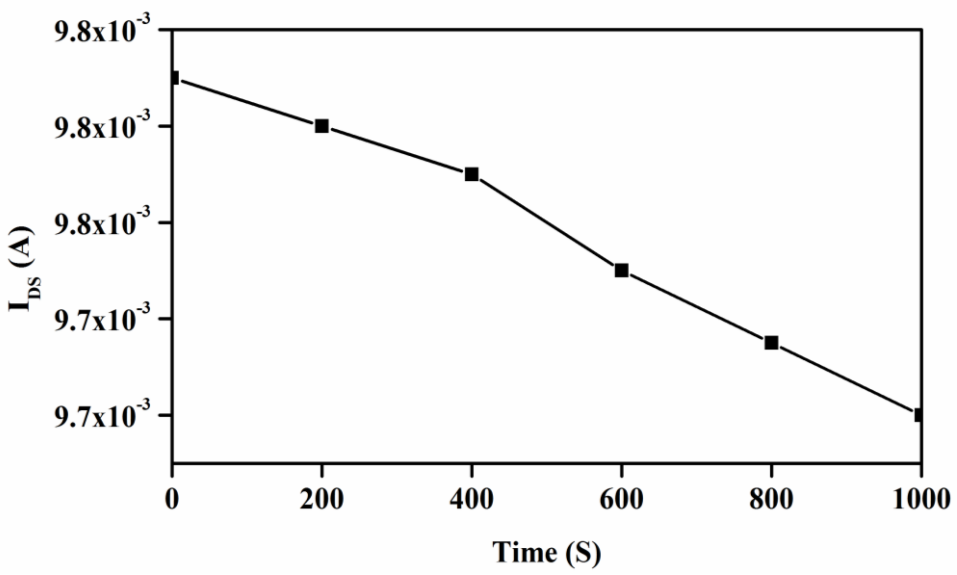


Figure 11. Time dependence of drain current under continuous gate bias.

In addition, as shown in Figure 12(a) and 12(b), the device showed little hysteresis between forward and reverse scans and their subthreshold swings were as low as 0.67 V/decade. Both low hysteresis and small subthreshold swings indicate that the heat treated Rubrene thin films have a low density of traps [23].

From an evaluation of 10 devices, it is observed that the overall characteristics of Rubrene device developed in this investigation are repeatable and their performance results shows good agreement with the data published in literature [24, 25].

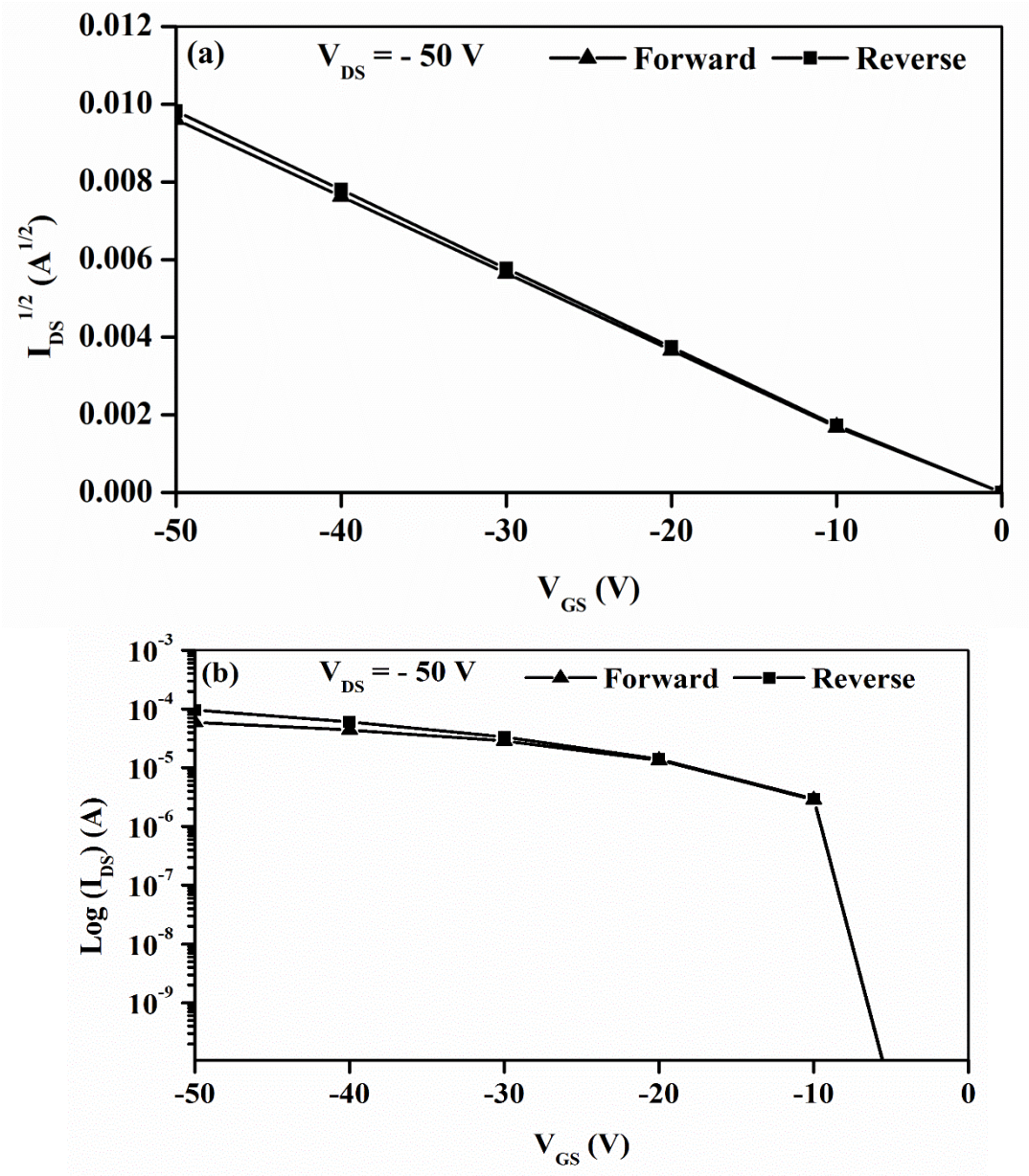


Figure 12. Transfer characteristics: (a) Log (I_{DS}) vs.V_{GS} (b) $\sqrt{I_{DS}}$ vs. V_{GS} scanned in the forward and reverse direction at the V_{DS} = - 50 V.

4.3.5 Need for OTS-SAM-Treatment of SiO_2

It is the general view that abrupt heat treatment would avoid the need for surface treatment in general. However, the results of this study have shown that surface treatment adds further value to the results attained with good heat treatment. A comparison of the results of sample S3 (OTS) of this study and the published data of H. M. Lee and co-workers [10] is presented in Table 7 to highlight the combined advantages of heat treatment and surface treatment. It can be inferred that heat treatment and surface treatment contribute for improved performance of the device for critical applications such as switching.

Table 7 Comparison of performance parameters of the present work with published data of Hyeok Moo Lee and co-workers [10]

Parameters	**Published data**	**Present work**
Materials		
Substrate	n+Si	n+Si
Dielectric	SiO_2 (100 nm)	SiO_2 (200 nm)
OSC	Rubrene (20 nm)	Rubrene (80 nm)
Gate	n+Si	Au
Source/Drain	Au	Au
Device parameters		
Channel Length	50 µm	30 µm
Channel Width	1000 µm	3000 µm
Heat treatment	170 °C for 1 minute	175 °C for 1 minute
Performance parameters		
I_{ds} (µA)	120	390
V_{gs} (V)	20	20
µ (cm^2/Vs)	1.21	1.36
V_{th} (V)	- 1	- 0.8
I_{on}/I_{off}	$>10^6$	10^7
S (V/dec)	0.62	0.59

Having studied the important features of the OFET's, the important results of the work are summarized in the conclusion section.

5. CONCLUSION

This study has shown that the developed OFET meets the requirements of FETs for switching applications, though the thickness would require reduction. The following are the important conclusions of this study:

i. The electrical performance of Rubrene based OFETs has strong correlation to the processing condition and nature of the active layer.
ii. The Rubrene thin film when subjected to heat treatment at 175°C for 1 minute transforms the amorphous state of Rubrene to crystalline state when formed on SiO_2/Si substrate.
iii. OTS-treatment alters the dielectric surface property of SiO_2 and this result in distinct enhancement of the structural order of the Rubrene thin film due to the reduction in surface free energy.
iv. Sample OFETs, S3 (OTS) has very high mobility of 1.36 cm^2/Vs and current on/off ratio of 10^7 with reduced threshold voltage as well as subthreshold swing which are ideal for switching applications.
v. Rapid heat treatment method at 175°C for 1 minute when combined with surface modification appears to be a more effective way of fabrication of high-performance OFETs and it is likely to offer better solutions for manufacturing as well as in switching applications.

ACKNOWLEDGMENTS

The authors are grateful to the CeNSE, Indian Institute of Science, Bengaluru for providing facilities and also JSSRF and NIE, Mysuru for their support and encouragement to S. Parameshwara for pursuing Ph.D. work.

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