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Optimization of 14nm Horizontal Double Gate for Optimum Threshold Voltage Using L9 Taguchi Method

N.H.N.M. Nizam[1], Afifah Maheran A.H[1*], F. Salehuddin[1], K.E. Kaharudin[2], and Noor Faizah Z.A.[3]

[1]Micro and Nano Electronic Research Group (MiNE), Faculty of Electronics and Computer Engineering, Universiti Teknikal Malaysia Melaka (UTeM), Hang Tuah Jaya, Durian Tunggal, 76100 Melaka, Malaysia
[2]Lincoln University College Main Campus, Wisma Lincoln, No. 12, 14, 16 & 18, Jalan SS 6/12, 47301 Petaling Jaya, Selangor Darul Ehsan, Malaysia
[3]Faculty of Architecture and Engineering Limkokwing University, Inovasi 1-1, Jalan Teknokrat 1/1 63000 Cyberjaya, Selangor, Malaysia

ABSTRACT

Silvaco ATHENA TCAD tools are used to model and simulate the electrical properties and characterization of the suggested layout of a 14 nm gate length (Lg) Double Gate Bilayer Graphene Field Effect Transistor (FET). Hafnium Dioxide (HfO_2) serves as the high-k material in the negative channel metal oxide semiconductor (NMOS) device, while Tungsten Silicide (WSi_x) serves as the metal gate. The investigated process parameters are threshold voltage (V_{TH}) adjustment implant dose, threshold voltage (V_{TH}) adjustment tilt angle, source/drain (S/D) implant tilt angle, and source/drain (S/D) implant dose, while the noise factors are threshold voltage (V_{TH}) adjustment implant energy and source-drain (S/D) implant energy. The device was optimized using the Taguchi approach, which incorporates L9 orthogonal arrays and analysis of variance (ANOVA). The most important elements impacting the V_{TH} are the S/D implantation dose. The value of the V_{TH} when compared to the original findings before the optimization is 0.204V, which is 7.059% lower than the desired value. The findings of the optimization procedure show excellent efficiency of the device with a V_{TH} of 0.191, which is 0.007% closer to the 2013 target set by the International Technology Roadmap Semiconductor (ITRS).

Keywords: Bi-GFET, MOSFET, Taguchi, threshold voltage (V_{TH})

1. INTRODUCTION

For decades, researchers and manufacturers have been working hard to overcome the problems and obstacles of enhancing the performance of semiconductor devices. One approach is to reduce the length of the device's channel in order to keep MOSFET's design is preserved while the device's performance and visibility are enhanced. [1]. The future growth of the semiconductor industry is contingent on researchers maintaining their track record of success in device scaling. The International Technology Roadmap for Semiconductors (ITRS) is an organization that studies the development path of devices in accordance with predetermined parameters such as physical size and architectural design. Since our design and size are documented in the ITRS, we used it as a point of reference while the International Roadmap Device and System (IDRS) examines the roadmap that is focused on FinFET and Gate All Around (GAA). This decade's forecast is laid out in the International Technology Roadmap for Semiconductors since our design and size are shown in the ITRS, which are planar, multi-gate (MG), and silicon on insulator (SOI). For most transistors, the whole electrical performance is determined by the channel length, making it a crucial parameter. The shorter the channel length in a transistor, the faster it can switch between its ON and OFF states, because the current has less distance to travel through the source and drain regions. High drain biases and a decrease in output resistance characterize channel length modulation. Increasing the width of a channel has the effect of decreasing its resistance and

* afifah@utem.edu.my

increasing the amount of current that can flow through it since resistance is inversely proportional to the square of the channel's length. Due to channel length modification in the saturation zone, the drain current will increase gradually as the drain-to-source voltage increases [2], [3].

Multi-gate (MG) MOSFET which is a double gate (DG) architecture is one of the potential solutions for furthering the reduction of the channel length while also having greater control over the channel [4]. Over the standard gate MOSFET, the DG MOSFET has several advantages, including a nearly perfect subthreshold slope, less intrinsic gate and junction capacitances, and a greater ON/OFF current ratio [5]. A high permittivity dielectric material is used in DG MOSFETs to improve the performance of the gate length, which results in improved overall performance. Two identical gates are anticipated to double the entire sum of electrons displayed within the channel region, resulting in an increment within the ionization potential. Recently, developments in the field of graphene, a two-dimensional carbon material with unique properties, have piqued the interest of many researchers. However, due to the absence of the band gap in monolayer graphene, its use in digital applications is restricted [6]. This leads to the introduction of bilayer graphene as a result of the feature that bilayer graphene would be the only suitable material to have an adjustable band gap [7].

The threshold and surface potentials of the model were discovered to be significantly influenced by simulated factors including oxide thickness, quantum capacitance, and channel length. As metal oxide semiconductor (MOS) devices get smaller, it becomes very hard to keep the amount of power used in the off-state constant. Thinner and shorter gate oxides are a trend in cutting-edge complementary metal oxide semiconductor (CMOS) technology [8], [9] The ON/OFF frequency ratio of a transistor could be enhanced by using a graphene channel. Graphene with doped bilayers has been proven to be suitable for use in ballistic transportation systems due to its lack of defects [10], [11]. The threshold voltage (V_{TH}) of a MOSFET is a crucial physical characteristic. V_{TH} is the threshold gate voltage at which a source-drain channel can be formed. The shape and electrical properties of a MOSFET device are sensitive to variations in dopant concentration, which can be influenced by dose, energy, tilt, and rotation. To further elaborate, an ideal nanoscale device with nominal threshold voltage and low leakage current (I_{OFF}) requires an accurate assessment of fluctuation in the input parameters of miniaturized devices.

In device characterization, designing, and circuit design, the threshold voltage V_{TH} of a MOSFET may be a critical electrical parameter to consider. It is additionally utilised in the advancement of devices, the control of processes, and the observation of reliability. The gate voltage is required to actuate an inversion layer within the channel of the device [12]. Additionally, using high-k dielectric allows for a larger gate capacitance at a greater thickness. [13]. It is possible to reduce SCEs and reduce leakage current by using a metal gate and high-K dielectric material. [14], [15]. In this study, the L9 Taguchi approach was used to optimise the process parameter fluctuations towards the V_{TH} value [16]. The Taguchi approach incorporates executing research to decide which input process elements have the greatest effect on device attributes. Faizah *et al*. (2017) demonstrated that the use of Taguchi makes a difference between researchers and creators in deciding which parameter has the most prominent effect on the execution of the device, thereby improving the general execution of the design [17]. Moreover, the Taguchi approach has been proven to generate significant products in a brief sum of time and at the most reduced conceivable fetched [18]. Due to its outstanding electrical properties and thermal stability, Tungsten Silicide (WSi_x) was chosen as the metal gate material in this study, with Hafnium dioxide (HfO_2) serving as the high-k dielectric permittivity in NMOS [19], [20]. G. Dhiman *et a*l. claim that the HfO_2-based device outperforms SiO_2 and Al_2O_3 because of channel depletion and enhanced fringing fields [21]. HfO_2 can thicken the oxide without modifying the surface possibilities, leading to lower drain current. By changing the gate-source voltage and the amount of doping in the substrate, the surface possibilities for the minimum oxide thickness can be enhanced. [22]. Metal-gate work function engineering proposed by Hong *et al*. patent allows WSi_x to be used as a metal gate since

it is compliant with both NMOS and PMOS devices. WSi_x, the metal-gate material, has a variable work function [23]. Titanium nitride (TiN) has a high melting point, excellent corrosion and diffusion resistance, and other benefits, but it also has a number of disadvantages. TiN has seen extensive use as the metal gate in MOSFETs, as it is found to be functional for p-MOSFETs. Nevertheless, the scope for adjusting the TiN work function is rather restricted [24], [25]. WSi_x was chosen because it can operate with both nMOS and pMOS transistors. Since HfO2/WSix has been extensively utilized in previous studies for device design, we proceeded with those materials and added the L9 orthogonal array Taguchi method to obtain a nominal threshold voltage [16], [20], [26], [27]. Single-layer-channel graphene field effect transistors with multi-layer contacts have a low contact resistance. This paper aims to capture the virtual fabrication design and demonstrating of four process parameters, known as threshold voltage (V_{TH}) adjustment implant dose, threshold voltage (V_{TH}) adjustment tilt angle, source/drain (S/D) implant dose, and source/drain (S/D) implant tilt angle, while the noise factors are threshold voltage (V_{TH}) adjustment implant energy and source drain (S/D) implant energy, in order to obtain the nominal value of V_{TH} of the proposed 14nm double gate Bi-GFET NMOS.

2. METHODOLOGY

2.1 Process Simulation of 14nm Bi-GFET NMOS

The ATHENA module of Silvaco TCAD tools has been used to simulate a 14 nm double gate n-channel Bi-GFET. The p-well region uses Boron as a dopant with a dose of $1.0x10^{14}$ ions/cm^3 and an 8nm p-type silicon substrate with a <100> orientation. In the channel region, the threshold voltage adjustment is implemented with boron dose of $1.13x10^{13}$ at 20KeV and tilted at 10º. Then, on top of the silicon, a bilayer graphene with a thickness of 1nm was deposited. In this study, hafnium dioxide (HfO_2) was used as a high-k dielectric with a permittivity of 22 [28]. A 2nm layer of HfO_2 was deposited on top of bilayer graphene, followed by a tungsten silicide (WSi_x). Etching is then used to achieve the desired thickness and the gate length of 14nm. The metal-gate work function of 4.5eV was assigned to the WSi_x gate [29]. To keep the V_{TH} feature, the efficient metal-gate work function had to be tweaked. Arsenic was injected at a dose of $1.00x10^{17}$ at 2KeV tilted at 77º for the source drain implant. Finally, to create the contacts, a layer of aluminum was applied to the structure and any extra aluminum was etched away. The transistor is then subjected to an electrical characteristic process using the ATLAS simulation module to study the threshold voltage of the device in relation to ITRS. The value of the threshold voltage for the 14nm gate length must be within 0.167V to 0.216V [30].

2.2 L9 Orthogonal Array Selection of the Process Parameters

Because of its simplicity and efficiency, the Taguchi method has been widely adopted as an optimization tool in numerous engineering processes. This is because the Taguchi method can determine the optimal value of process parameters for a specific process or design. The L9 orthogonal array Taguchi method was chosen to optimize the process parameter fluctuations towards the V_{TH} value to attain the perfect device performance of the 14nm double gate n-type MOSFET. Faizah *et al*. was using the L9 (34) OA, which has four columns and nine rows, to optimize the process parameters in order to reach a nominal value for the V_{TH} [13]. In this research four control factors and two noise factors were chosen based on the established research papers [31]. The control factors selected in this study are threshold voltage adjust implantation (A), threshold voltage tilt angle (B), S/D implantation (C), and S/D tilt angle (D), while the noise factors are threshold voltage energy and S/D energy. The parameters are taken from the previous researcher and show a good agreement to obtain the nominal threshold voltage [19], [32], [33]. This is a technique that is used in the Taguchi method. It shows a range of values so that the best one can be chosen. The dose is varied until the nominal threshold voltage is obtained for example,

the best value for V_{TH} adjust implantation was 1.23x1013. Table 1 shows the values of each parameter at various levels, while Table 2 shows the noise factors for n-type MOSFETs.

Table 1 Process Parameters and their levels

Symbol	Process Parameters	Unit	Level 1	Level 2	Level 3
A	V_{TH} adjust implantation	Atom/cm^3	1.03x10^{13}	1.13x10^{13}	1.23x10^{13}
B	V_{TH} tilt	Degree	8	10	12
C	S/D implantation	Atom/cm^3	0.80x10^{17}	1.00x10^{17}	1.20x10^{17}
D	S/D tilt	Degree	75	77	79

Table 2 Noise factors and their levels

Symbol	Process Parameters	Unit	Level 1	Level 2
X	V_{TH} energy	KeV	18	20
Y	S/D energy	KeV	1.8	2

3. RESULTS AND DISCUSSION

3.1 Fabrication Simulation Result

Silvaco TCAD tools were used to perform electrical properties on a 14nm n-channel double gate Bi-GFET. Device for 14 nm n-type double gate Bi-GFET is shown in Figure 1, which is the finalized device. Since the type of gate was changed, there was a difference in the amount of doping incorporated into the device. Figure 1 depicts the silicon, Bilayer graphene, High-K/Metal Gate, and aluminum layouts of this 14 nm HfO_2/WSi_x double gate Bi-GFET.

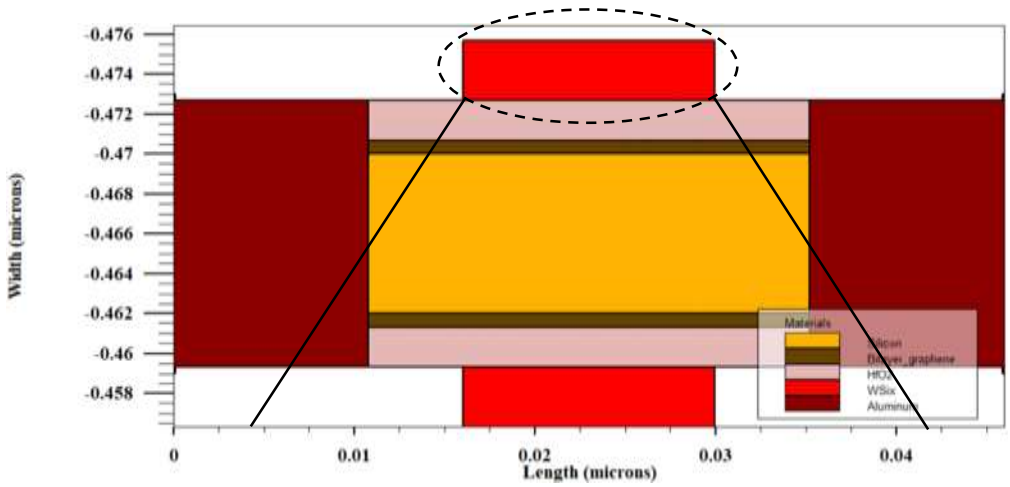

Figure 1. Competed device of 14nm Bi-GFET NMOS.

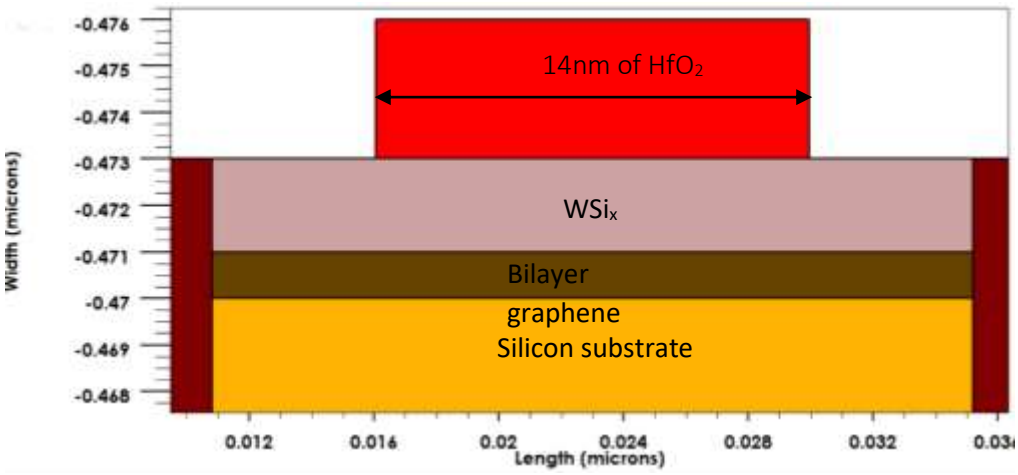

Figure 2. Measurement of the metal gate and completed device.

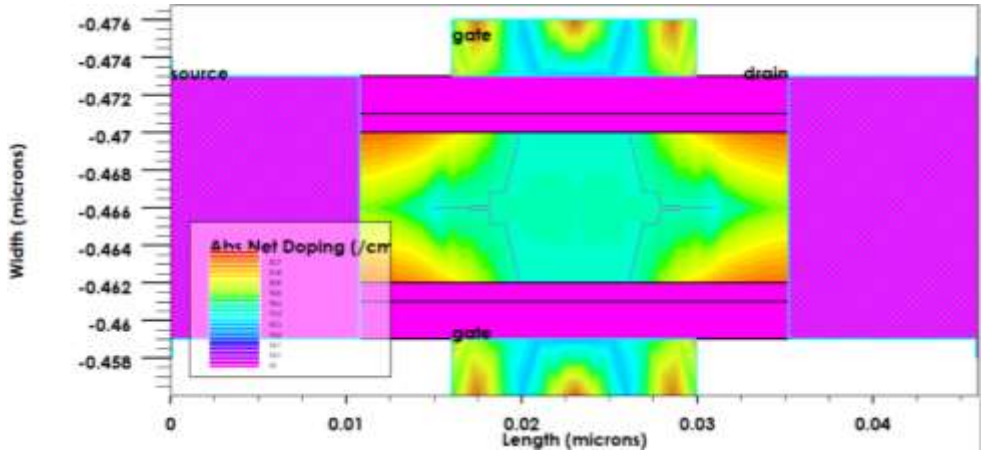

Figure 3. The doping profile of 14nm Bi-GFET NMOS.

3.2 Characterization of the NMOS Device

The Atlas module was used to analyse the 14 nm horizontal double gate Bi-GFET NMOS device's properties. Figure 4 shows the results of a sequential application of drain currents vs gate voltages. During the simulation, the drain voltage of VDD is maintained at 0.5 V, while the gate voltage of VGS is increased from 0 V to 1 V in serial steps of 0.05 V. VTH = 0.204737 V, as depicted in the graph, is in line with the 2013 forecast provided by the International Technology Roadmap for Semiconductors (ITRS). Figure 5 is a plot of drain current (IDS) versus drain voltage (VDS) for the device with VG set to 0.5 V and 1.0 V.

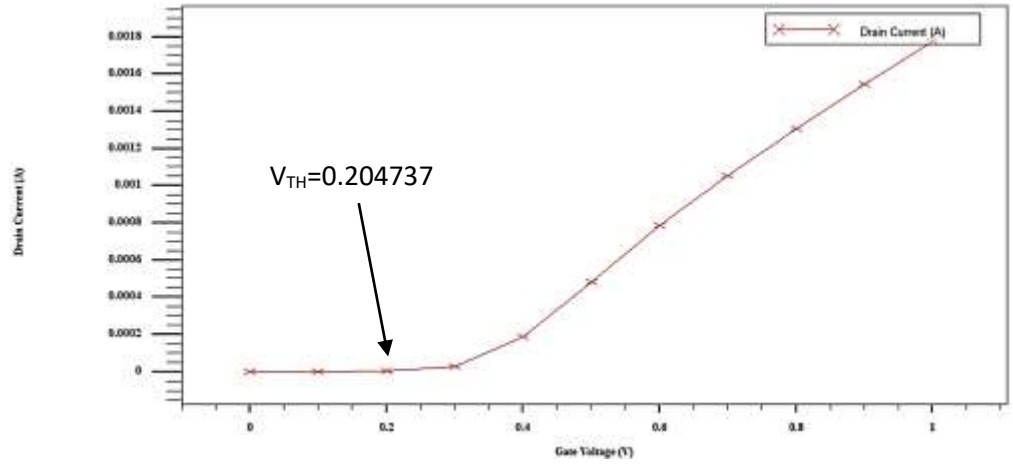

Figure 4. Drain current (IDS) versus Gate voltage (VGS)

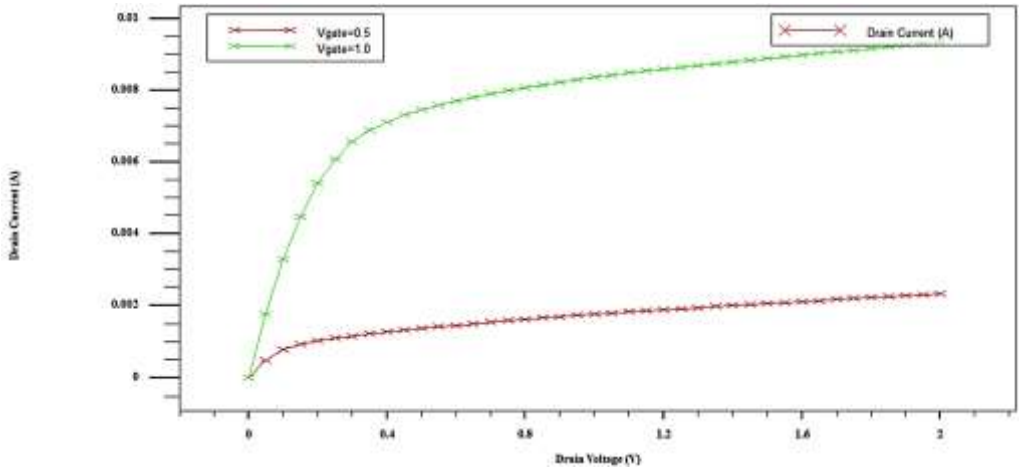

Figure 5. Drain Current (IDS) versus Drain Voltage (VDS).

3.3 Signal-to-Noise Ratio Analysis

To optimize the threshold voltage, the Taguchi L9 Orthogonal array method was used in this study. In this study, the nominal is the finest feature of the V_{TH}. Since the ITRS specifies a multi-gate device, the Taguchi analysis technique has been employed to derive an adjustment factor and a dominant factor. Adjusting the values of the process parameters based on the adjustment factor allows for the attainment of the desired threshold voltage. To get a better understanding of the device's characteristics, the following phase was to recognize the control variables that have the most prominent effect to the device. The SNR investigation of the exploration is one of the processes. In this experiment, the V_{TH} investigation is alluded to as SNR which is nominal the best (NTB) where the objective of the investigation is to investigate the control factor level that provide a result esteem that is near to or the same as the anticipated esteem, which is 0.191V. On the off chance that a factor which is a process parameter has the most elevated signal to noise ratio, it is expected that it incorporates a superior signal than the irregular impacts of the noise variables. To attain the nominal V_{TH} value predicted by ITRS, the best nominal quality characteristic type was selected in this study. The results of optimizing the V_{TH} of the NMOS transistor using the L9 Orthogonal array method are shown in Table 3 below.

Table 3 Threshold Voltage (V_{TH}) value based on the L9 Orthogonal Array

Exp No.	Threshold Voltage, V_{TH} (V)				OV Mean	SNR
	X1, Y1	X2, Y2	X2, Y1	X2, Y2		
1	0.188	0.204	0.185	0.202	26.01	26.12
2	0.186	0.204	0.184	0.203		24.95
3	0.186	0.206	0.183	0.203		24.50
4	0.187	0.204	0.185	0.201		26.30
5	0.202	0.227	0.199	0.225		23.21
6	0.189	0.205	0.187	0.203		26.52
7	0.191	0.218	0.188	0.217		21.97
8	0.189	0.199	0.187	0.197		30.23
9	0.200	0.210	0.197	0.208		30.28

The dominant and adjustment factor for NMOS transistors must be determined next. Table 4 summarizes the findings of the V_{TH}. S/D Implantation (C) has the greatest influence on V_{TH} (55%) in the NMOS device, so it was chosen as the dominant factor. On the other hand, S/D tilt angle (D) has the second highest impact on variance (17%) but the highest Mean score (41.57%). As a result, the adjustment factor was set as parameter D. Then, to get the V_{TH} value close to the ITRS 2013 prediction, parameter D was altered from 73° to 80°.

Table 4 Signal Noise Ratio (SNR) level of Process Parameters

Symbol	SNR (dB)			Factor Effect (%)	
	Level 1	Level 2	Level 3	Variance	Mean
A	25.19	25.35	27.49	16	20.93
B	24.80	26.13	27.10	13	2.68
C	27.63	27.18	23.23	55	34.81
D	26.54	24.48	27.01	17	41.57

Table 4 shows the SNR NTB of the experiment. The values of the dashed flat lines within the graph represent the values of the overall mean of the SNR (NTB), which is 26.01 dB. In addition, the level values for each process parameter are presented on a graph. According to the graph, it is obvious that the levels of calculated SNR, which are A3 (27.49 dB), B3 (27.10 dB), C1 (27.63 dB), and D3 (27.01 dB), were the optimum process parameters for the nominal the better.

3.4 Analysis of Variance (ANOVA)

The analysis of variance (ANOVA) is a widely used factual strategy for determining which of the input process parameters had a significant influence on the execution characteristic under investigation [34]. To put it simply, it computes parameters such as the sum of squares (SSQ), the degree of freedom (DF), the variance, the F-value, and the percentage of each factor that is present. The standard deviation of the test data from the mean value of the data is calculated. Table 5 depicts the results of the ANOVA for the device under evaluation. The percentage of the factors' impact on SNR demonstrates which process parameters are the most overwhelming. Regarding factor effect on SNR, the results demonstrate that the S/D implantation has the biggest impact on the nominal value of the V_{TH}, with a 55% influence, followed by the S/D tilt angle, which

has a 17% influence. The percentage effect on the SNR for the V_{TH} adjust implantation and V_{TH} tilt angle is lower, with 16% and 13%, respectively, for the V_{TH} adjust implantation and V_{TH} tilt angle.

Table 5 Analysis of Variance for threshold voltage (V_{TH})

Symbol	Sum of Square (SS)	Mean Square	Factor Effect (Mean) (%)	Factor Effect on SNR (%)
A	10	5	20.93	16
B	8	4	2.68	13
C	35	18	34.81	55
D	11	5	41.57	17

3.5 Confirmation Test

According to Table 6, the 14nm double gate Bi-GFET device was virtually constructed using the optimal process parameters levels predicted by the L9 OA of the Taguchi technique, which are listed in Table 6. For V_{TH}, the highest S/N ratio for factor A was at level 3 (27.49 dB), the highest for factor B was at level 3 (27.10 dB), the highest for factor C was at level 1 (27.63 dB), and the highest for factor D was at level 3 (27.01 dB). Since factor D was set as an adjustment factor in the ANOVA, the tilt angle value was swept. To achieve the best V_{TH}, the best combination factors are A3, B3, C1, and D3. According to Table 6, the 14nm double gate Bi-GFET device was virtual fabricated utilizing the optimized process parameters levels anticipated by the L9 OA of the Taguchi strategy, which are recorded within the Table 6. Table 7 shows the results, which illustrate that the nominal V_{TH} value was 0.191V, with an SNR for NTB of 30.53 dB (still within the range of 28.23 to 32.83) and an SNR for mean of -14.35 (still within the range of -12.05 to -16.65). This obviously demonstrates that the L9 OA of the Taguchi approach has effectively optimized all the method parameters.

Table 6 Best setting parameter for V_{TH}

Symbol	Process Parameter	Level	Unit	Best Value
A	V_{TH} adjust implantation	3	Atom/cm^3	1.23x10^{13}
B	V_{TH} tilt	3	Degree	12
C	S/D implantation	1	Atom/cm^3	0.80x10^{17}
D	S/D tilt	3	Degree	79

Table 7 Confirmation results for V_{TH} using L9 OA of Taguchi Method

Threshold Voltage (V_{TH})			Best Value		
X1, Y1	X1, Y2	X2, Y1	X2, Y2	Mean	NTB
0.191	0.202	0.189	0.199	-14.35	30.53

Table 8. Simulation Results of 14nm Bi-GFET double gate

Performance Parameter	ITRS Prediction	Non-Optimized results	Optimized results
V_{TH} (V)	0.191 ±12.7 %	0.205	0.191

4. CONCLUSION

In this study, the L9 OA Taguchi approach is a reliable approach for optimizing the process parameters in the development of a 14nm n-type double gate MOSFET utilizing Bilayer graphene, high-k/metal gate technology to attain the nominal value of the threshold voltage predicted by the ITRS 2013. As was previously mentioned, the ITRS examines device progress according to predetermined criteria including size and layout. The ITRS was beneficial since it detailed our design's double gates and 14 nm size, while the International Roadmap Device and System (IDRS) examined the roadmap through the view of FinFET and Gate All Around (GAA). In next projects, we'll be developing technology that's in line with the semiconductor industry's most recent roadmap. According to this experiment, S/D implantation are the most critical attributes in obtaining an optimal V_{TH} value. Only a small variation in the dopant value, however, will have a significant impact on the overall performance of the device.

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