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A 12 GHz LC-VCO Implemented with S' shape Inductor using Silicon-on Sapphire Substrate

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ABSTRACT

A voltage-controlled oscillator (VCO) is an electronic oscillator whose oscillation frequency is controlled by a voltage input. In a VCO, low-phase noise while consuming less power is preferred. The tuning gain and noise in the control signal produce phase noise; more noise or tuning gain implies more phase noise. Sources of flicker noise (1/f noise) in the circuit, the output power level, and the loaded Q factor of the resonator are all crucial factors that influence phase noise. As a result, creating a resonator with a high Q-factor is essential for improving VCO performance. As a result, this paper describes a 12 GHz LC Voltage-Controlled Oscillator (VCO) employed with a 'S' shape inductor to improve phase noise and power performance. The phase noise for the VCO was reduced using a noise filtering technique. To reduce substrate loss and improve the Q factor, the inductor was designed on a high-resistivity Silicon-on-Sapphire (SOS) substrate. At 12 GHz, the optimised S' shape inductor has the highest Q-factor of 50.217. At 10 MHz and 100 MHz, the phase noise of the 12 GHz LC-VCO was -131.33 dBc/Hz and -156.71 dBc/Hz, respectively. With a 3.3 V power supply, the VCO core consumes 26.96 mW of power. Based on the findings, it is concluded that using an 'S' shape inductor in the VCO circuit will enable the development of low-cost, high-performance, very low-power system-on-chip wireless transceivers with longer battery life.

Keywords: Inductor, Q-factor, Silicon-on sapphire, Voltage controlled oscillator, phase noise

1. INTRODUCTION

Voltage-Controlled Oscillators (VCOs) are essential components of wireless and optical communications transceivers. The primary challenge in VCO design is to minimise phase noise while consuming the least amount of power, which can be accomplished by improving the low Q-factor of the inductors [1]. The performance of a VCO can be measured using specifications such as power consumption, phase noise, and oscillation frequency.

Furthermore, with rising performance requirements for phase noise, power, and tuning range, fully integrated LC voltage-controlled oscillators are becoming increasingly important in radio-frequency wireless network systems. Significant work has been conducted in optimizing the LC tank and negative resistance cells to improve phase noise and power performance [2][3][4]. To reduce power consumption and improve phase noise in VCO circuits, higher Q-factor inductors with high self-resonance frequency (SRF) are required.

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Instead of using a high Q-factor LC tank, filtering techniques are also used [5] to reduce the excess noise contribution from the active current source. In contrast, the on-chip inductors have been adopted as a tail current source in the VCO core. This paper adopts this filtering technique to improve VCO's phase noise performance and power consumption. It also showed that the suggested Inductor is been monolithically incorporated with an LC VCO in order to analyze the effect of this high Q-factor Inductor on VCO performance.

2. DESIGN OF VCO CIRCUIT

The LC oscillator has several potential benefits, including symmetry, lower phase noise, and higher transconductance. Because of these benefits, this oscillator was chosen to design the 12GHz VCO. Figure 1 represents the schematic of an LC-VCO operating at 12GHz that uses noise filtering. A schematic of 12GHz LC-VCO is adapted from [6]. A pair of cross-coupled PMOS and NMOS transistors, which produce the necessary negative impedance to counteract the losses of the LC tank, is the main part of this VCO. The cross-coupled transistors supply the energy lost due to the LC tank's parasitic resistance, which offers a negative resistance.

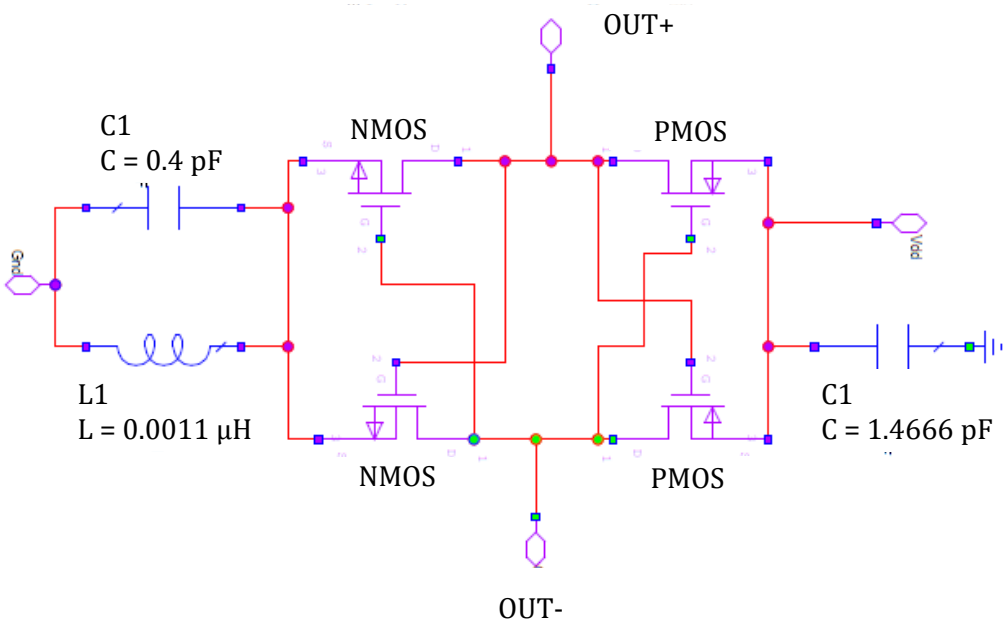


Figure 1. LC-VCO Topology.

To ground the second harmonic content of drain current noise, the noise filtering technique employs LC combination [7]. The inductor and capacitor filter are placed at the switching pair's common source point to resonate in parallel with the capacitance at node $2\omega_0$. The second harmonic current is thus prevented from flowing to ground via the resonator and switching transistor. The noise filter circuit operates as if it were biassed by a tail-current source that consumes zero voltage headroom while producing the maximum achievable amplitude. [6]. As a result, the phase noise in this topology has been reduced. A LC-VCO is made up of two basic blocks, as shown in Figure 2, an active circuit and a resonator. R_{tank} is the LC tank loss, and -R is the active circuit's effective negative resistance compensating for tank losses.

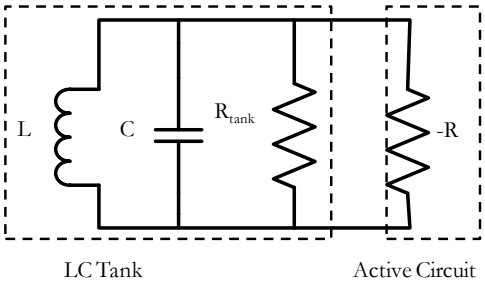


Figure 2. LC Oscillator Model.

The negative resistance of the cross-coupled pair is given by -2/gm, where gm is the transconductance[8]. The condition in (1) yields the minimum value of transconductance (gm) of a cross-coupled transistor for oscillation [8].

$$\frac{2}{g_m} \geq R_p \tag{1}$$

Where is a loss of the resonators and given by (2),

$$R_p = 2\pi fQL \tag{2}$$

Where L is the inductance, f is the frequency, and Q is the resonator's quality factor. An 'S' shape inductor and an NMOS varactor are used to construct the LC tank. The NMOS varactor is also an important factor in determining VCO performance. Two NMOS varactors are used in the tank for tuning in this configuration. The top biassed VCO with the large shunt capacitance (C1) connected in parallel with the PMOS and the second harmonic filter comprising the parallel inductance L1 and capacitance C2 with high reactance at the second harmonic were used to minimise extra phase noise [9]. As presented in Figure 3, the Inductor in the LC tank is replaced with an S' shape inductor. This inductor is connected in parallel with two NMOS varactors (S1-S2) to achieve a 400 MHz tuning range with tuning voltages ranging from 0 V to 3 V.

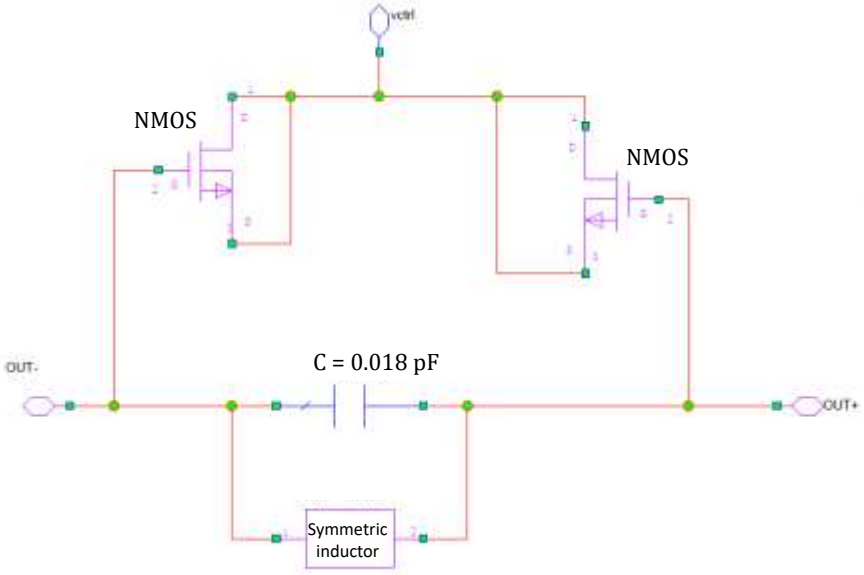


Figure 3. LC tank.

3. The LC Tank Optimization

As shown in Figure 2, the LC oscillator is composed of an inductor (L) and a capacitor (C). The LC oscillator generates the sinusoidal signal by charging and discharging L and C. The R_{tank} simulates resistive loss in the tank, where it stores energy and controls the oscillator's frequency. The -R model represents the active circuit that compensates for tank losses.

The oscillating frequency of oscillators is f_0, and at f_0, the impedance of the L and C are equal in magnitude and opposite in polarity, as given by Equation (3).

$$\frac{1}{2\pi f_0 C} = 2\pi f_0 L \tag{3}$$

After simplifying Equation (3), the f_0 can be obtained as given by Equation (4).

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \tag{4}$$

In an LC tank shown in Fig. 2, the tank's quality or energy efficiency is specified in terms of Q-factor and is defined by Equation (5), where ω=2πf.

$$Q = \frac{\omega(\text{energy stored})}{(\text{average power dissipated})} \tag{5}$$

However, the phase noise of LC-VCO is inversely proportional to the square of the Q_{tank}. The phase noise is described by Leeson as shown in Equation (6) [4]:

$$L\{\Delta\omega\} = 10\log\left[\frac{2FkT}{P_s}\cdot\left[1+\left(\frac{\omega_0}{2Q_L\Delta\omega}\right)\right]^2\cdot\left(1+\frac{\omega_{\frac{1}{f^3}}}{|\Delta\omega|}\right)\right] \tag{6}$$

Where *F* is a noise factor, *k* is Boltzmann's constant, *T* is the absolute temperature, P_s is the average power dissipated in the resistive part of the tank, ω_0 is the oscillation frequency, Q_L is the loaded Q-factor of the tank, Δω=2πf is the offset from the carrier, and ω^{1/f^3} is the flicker noise corner frequency between $1/f_3$ and $1/f_2$ at low offset frequencies [4]. Regarding (6), using a high Q-factor LC tank is the most effective way to lower phase noise. It is clearly shown that phase noise has an inverse relationship with the power wasted in the resistive component of the tank. Therefore, enhancing the Q-factor of an inductor is an effective solution to improve the phase noise directly. Adding an inductor with a high Q-factor can decrease these noises, proving that smaller transistor sizes are no longer necessary to achieve low phase noise.

4. INDUCTOR DESIGN

The Q-factor is a parameter that characterises power loss in an inductor or measures its ability to save energy. The Q-factor is determined by the geometry of the inductor and the interconnect metal (copper (Cu), gold (Au), or aluminium (Al) [10]. The spiral inductor model, as shown in Figure 4(a), can be used to determine an inductor's Q-factor [11].

Figure 4. S' shape Inductor.

Where L_s represents the coil's equivalent inductance, R_s represents the equivalent resistance caused by the coil metal and effects caused by the conductor and substrate, C_s represents equivalent capacitance due to inter-turn capacitance, fringing capacitance, and capacitance due to coil metal overlaps with the underpass metal layers, and C_{ox} represents the capacitive effect of the oxide layer. R_{sub} and C_{sub} are the substrate's resistance and parasitic capacitance, respectively. The ohmic losses in the substrate caused by the displacement currents induced in the substrate are accounted for by R_{sub}, and Csub models the capacitive effects of the substrate. The Q-factor of an inductor is associated to the related causes of substrate loss and self-resonance factors, according to Equation (7). The substrate loss factor represents the energy dissipated in the silicon substrate, lowering the inductor's Q-factor. According to Equation (7), the Q-factor is inversely proportional to R_s, implying that Rs affecting the Q-factor of inductor metal losses.

$$Q_{factor} = \frac{\omega L_s}{R_s} \cdot \begin{pmatrix} \text{substrateloss} \\ \text{factor} \end{pmatrix} \cdot \begin{pmatrix} \text{self - resonance} \\ \text{factor} \end{pmatrix} \tag{7}$$

Inductors' geometrical parameters are optimized to improve the Q-factor and operating frequency range, which reduce losses caused by the two primary loss mechanisms, ohmic loss and substrate loss. Figure 4 (b) depicts an 'S' shape inductor design in which the outer diameter (OD), the width of metal traces (W), and the thickness of metal (T) are important geometrical parameters used to optimize to attain a high Q-factor of the Inductor. The 'S' shape topology, as shown in Figure 4 (b), consists of two semi-circles that do not enclose an area and form the letter 'S.' Furthermore, this S' shape inductor topology is suggested to reduce the resistance and the length of the metal tracks, allowing for a high Q-factor of the Inductor to be realized.

Table 1 S' shape Inductor with Very Optimize Parameter

Parameter	Optimization of S' shape Inductor
Metal Thickness (μm)	5.00
Metal Width (μm)	15.00
Outer Diameter (μm)	320.00
Q_{max}	50.22
Frequency (GHz)	12.00
Inductance (nH) @ Qmax	0.505
Resistance (nΩ) @ Qmax	0.758

The optimized S' shape inductor is summarised in Table 1. The metal thickness of 5 μm, metal width of 15 μm, and outer diameter of 320 μm are the optimum parameters for this 0.505 nH S' shape inductor, resulting in a Q-factor of 50.22 at 12 GHz. The S' shape inductor is implemented as a two-port network with the 12GHz LC-VCO, with the S-parameter characterising the inductor's electrical properties. In Figure 5, the S' shape inductor is modelled by a two-port network which is internally connected by a voltage (V) and current (I) (I). The input current and voltage are represented by I_1 and V_1, respectively, while the output current and voltage are represented by I_2 and V_2. This two-port linear network is assumed to have no independent energy sources and to be at rest at the start.

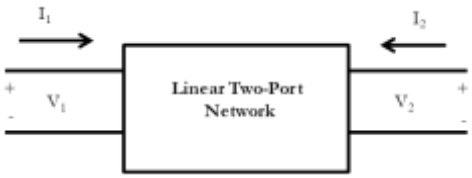


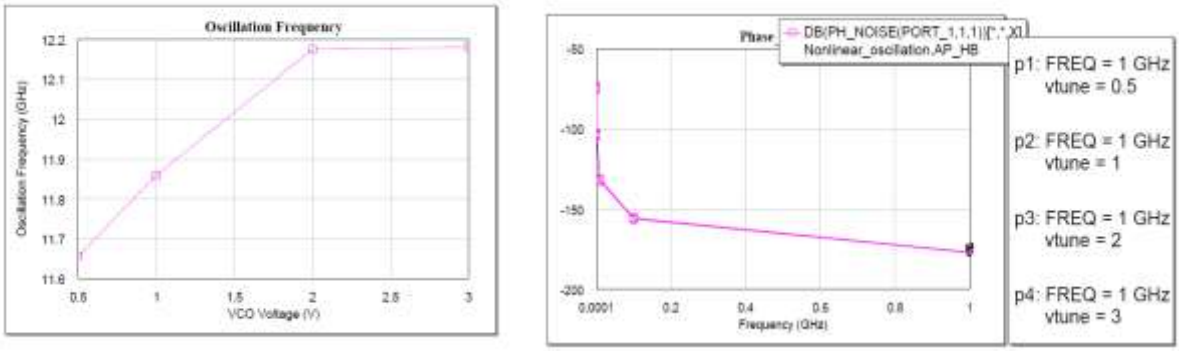
Figure 5. A General Two-Port Network with Voltages and Currents.

5. RESULTS AND DISCUSSION

A study on 12GHz LC-VCO performances using S' shape inductors is analyzed. The S' shape inductor is implemented in the LC tank of VCO as part of the resonator. This Inductor is placed in parallel with two NMOS varactors, as shown in Figure 1 (b), which is used to achieve an approximately 400 MHz tuning range with tuning voltage varied between 0V and 3V. The tuning characteristics of the presented 12GHz LC-VCO implemented with an S' shape inductor are plotted in Figure 7 (a). This VCO is tuned from 0 V to 3 V, which gives the frequency range between 11.6 GHz and 12.2 GHz.

The performance of 12GHz LC-VCOs with S' shape inductors is analyzed. The S' shape inductor is implemented as part of the VCO's resonator in the LC tank. This Inductor is connected in parallel with two NMOS varactors, as shown in Figure 3, to achieve a tuning range of approximately 400 MHz with tuning voltages varying from 0V to 3V. Figure 6 (a) depicts the tuning characteristics of the presented 12GHz LC-VCO with an S' shape inductor. This VCO is tuned from 0 V to 3 V, resulting in a frequency range of 11.6 GHz to 12.2 GHz.

The results show that a 12GHz LC-VCO with an S' shape inductor attains phase noise of -131.33 dBc/Hz at 10 MHz and -156.71 dBc/Hz at 100 MHz offset frequencies, respectively. The operating frequency of 12GHz is achieved at about 1.5 V of the tuning voltage. The phase noise performance of this VCO for offset frequencies ranging from 0.0001 MHz to 1 GHz is shown in Figure 6 (b). Figure 8 depicts the VCO's time-domain output.



(a) (b)

Figure 6. Phase Noise and Oscillation for 12 GHz VCO

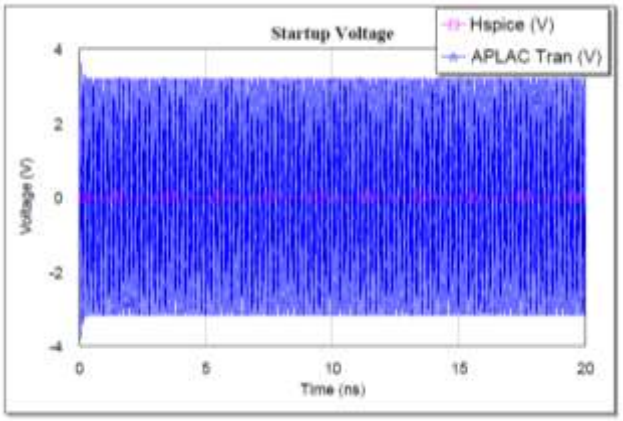


Figure 7. Time Domain Output of VCO

6. CONCLUSION

This paper demonstrated a potential solution for improving the performance of CMOS inductors and their associated circuit. This study used a cross-coupled VCO with an S' shape inductor and a noise reduction technique to reduce phase noise. The phase noise of the 12 GHz LC-VCO was -131.33 dBc/Hz and -156.71 dBc/Hz, respectively, at 10 and 100 MHz offset frequencies. The VCO core consumes 26.96 mW of power with a 3.3 V power supply.

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REFERENCES

[1] IEEE Std 802.15.4TM-2006, The Institute of Electrical and Electronics Engineers (IEEE), New York, 2016.
[2] A. Hajimiri and T.H. Lee, Design issues in CMOS differential LC oscillators, IEEE J. Solid-State Circuits, vol. 34, no. 5, (1999)pp. 717–724.

[3] A. Hajimiri and T.H. Lee, A general theory of phase noise in electrical oscillators, IEEE J. Solid-State Circuits, vol. 33, no. 2,(1998) pp. 179–194.
[4] T.H. Lee, The Design of CMOS Radio-Frequency Integrated Circuits, Cambridge Univ. Press, 1998.
[5] H.-C. Chiu, C.-S. Cheng, Y.-T. Yang, and C.-C. Wei, A 10 GHz low phase-noise CMOS voltage-controlled oscillator using dual-transformer technology, Solid. State. Electron., vol. 52, no. 5 (2008), pp. 765–770.
[6] E. Hegazi, H. Sjoland, and A.A. Abidi, A filtering technique to lower LC oscillator phase noise, IEEE J. Solid-State Circuits, vol. 36, no. 12 (2001), pp. 1921–1930.
[7] S. Bao and L. Li, A 10GHz CMOS VCO with Low Phase Noise. ASME Press, 2010.
[8] M. Rahimi, S.S. Jamuar, M.N. Hamidon, M.R. Ahmad, S.A. Mousavi, and M. Bayat, An optimized 2.4 GHz VCO circuit design and simulation with high-Q MEMS LC-tank, AEU - Int. J. Electron. Commun., vol. 64, no. 5 (2009), pp. 413–424.
[9] A. Grebennikov, Noise Reduction technique, RF Microw. Transistor Oscil. Des., vol. John Wiley, 2007.
[10] K.B. Ashby, I.A. Koullias, W.C. Finley, J.J. Bastek, and S. Moinian, High Q inductors for wireless applications in a complementary silicon bipolar process, IEEE J. Solid-State Circuits, vol. 31, no. 1 (1996), pp. 4–9.
[11] Z. Zhengyuan, W. Zhiyu, X. Shilu, Z. Zhengfan, C. Gang, and H. Shanglian, Optimization of Q factor in spiral inductor on silicon, in 6th International Conference on Solid-State and Integrated-Circuit Technology, vol. 1,(2001) pp. 251–254.