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Virtual Fabrication of 14nm Gate Length n-Type Double Gate MOSFET

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ABSTRACT

Due to Moore's law that predicted the channel length of a metal-oxide-semiconductor Field Effect Transistor (MOSFET) will tend to shrink from the submicron to the nanoscale size. Thus, precision in the manufacturing process has become crucial. This study describes the virtual fabrication as well as the electrical characteristics of a 14nm NMOS double gate with a bilayer graphene/high-K/metal gate. In this device, Hafnium Dioxide (HfO2) is employed as a high-k material, and Tungsten Silicide (WSix) is used as a metal gate. Several Silvaco TCAD Tools, including ATHENA and ATLAS, were utilized in the fabrication and simulation of the device, respectively. According to the simulation results, the optimal threshold voltage (V_{TH}), drive current (I_{ON}), and leakage current (I_{OFF}) and subthreshold slope (SS) values are 0.2059 *V,* 797.5650 *μA/μm. 29.5794 nA/μm, and 89.1712x10^{-3} V respectively. The findings of this research showed that the efficiency of this 14nm double gate n-type MOSFET device is satisfactory because the threshold voltage and leakage current parameters are in accordance with ITRS 2013, and that it may have been utilized as a utility man in future modelling and optimization efforts.*

Keywords: Bilayer Graphene, Double gate-MOSFET, High-K/Metal gate

1. INTRODUCTION

For decades, complementary metal oxide semiconductor (CMOS) down-scaling has followed Moore's law, with distinct sections of the transistor's design reducing by a constant factor to achieve good efficiency of power consumption [3]. The workhorse of the IC industry has been planar bulk MOSFET technology. However, due to the short channel effect (SCE), the scaling limit of typical planar bulk MOSFETs is nearing. Therefore, electrostatic control is required to combat SCE, which necessitates extremely high channel doping concentrations and ultra-thin gate oxide, leading in reduced channel mobility and gate leakage performance [4]. To resolve this concern, several novel semiconductor approaches have been suggested, including substituting SiO_2/polysilicon with a high-k/metal gateThe double gate (DG) with single material concept is a new device design that suppresses the short channel effect in a particular perspective. Due to its superior device scalability, DG MOSFETs are highly suited for CMOS circuit applications that require technology beyond 45 nm range in size. In a DG MOSFET, short channel effects, junction capacitance, and dielectric isolation are all reduced [5]. In n-channel horizontal double gate MOSFETs, a dielectric material with a high permittivity improves power dissipation and reduces leakage current The inclusion of two identical gates is expected to double the total amount of electrons in the channel region, resulting in increased I_{ON}. The current International Technology

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Roadmap Semiconductor (ITRS) report predicts the use of double-gate MOSFETs with high-k/metal gate technology to further increase the I_{ON} for high power multi gate technology [6]. The ITRS 2013 report is the most recent CMOS technoligy reference, according to the semiconductor roadmap, and it states that the 14 nm scale is still available. FinFET technolgy, for example, is the suject of the different technology and listed to different roadmap report.

The design of a double gate 14nm n-type transistor in our research is based on the well-known planar 14nm transistor, as described in the paper [7]. Due to the obvious greater screening effect of high-k materials, charged impurity scattering can be reduced, and the charge control of the channel can be improved due to the larger gate capacitance of high-k materials. In this research, we used the same high-k metal gate material, which is Hafnium Dioxide (HfO2) as a high-k, which is great in terms of electrical and thermal qualities, while Tungsten Silicide (WSix) as a metal gate which has a configurable work function [8], [9]. According to research, the high permittivity of High-K dielectrics, such as those derived from Hafnium-based materials, has outstanding electrical attributes. It is assumed that HfO_2 has a higher effectiveness when handling short-channel effects such as leakage current, I_{ON}/I_{OFF} ratio, and a variety of other factors. This is beneficial in terms of achieving low leakage current [7]. High-K dielectrics enable the physical thickness of the gate oxide to enhance while keeping the equivalent oxide thickness (EOT) constant, preventing gate tunnelling [10].

Graphene, among several novel materials, has received a great deal of focus in recent years because of its outstanding electrical properties [11]. High charge carrier mobility, high charge carrier density, great thermal conductivity, and high resilience have all been observed for intrinsic graphene [12]. However, graphene field effect transistors, despite its amazing electrical properties, are difficult to utilize in digital logic because graphene does not possess a band gap in their natural form, making them impossible to turn off. The use of graphene is very beneficial because, before the graphene transistors are made, it will be easier to predict how they will work at the circuit level. This will help to make high-performance devices at a lower cost [13]. As a result, bilayer graphene will be employed to measure this challenge in this study. The graphene channel in the transistor can generate a band gap with this method, resulting in a greater on-off ratio [11], [14]. Theoretically, bilayer graphene has been widely investigated and found to be thermodynamically stable [15].

1.1 Double Gate Architecture

Since the industry has been moving down to the 5nm technology node with non-planar devices, 14 nm is still in research since few researchers are still undertaking this work and yet it is still being used in the industry. Double gate MOSFET is based on CMOS technology. However, the technologies employed by GAA and FinFET are quite distinct from one another. GAA and FinFET are not based on CMOS technology. So, despite the fact that GAA nanowires are getting smaller, they are still difficult to manufacture and the procedure is not always the same. In addition, in this research, we are designing and optimizing a 14 nm double gate n-type MOSFET with utilizing combination gate material of graphene, HfO_2 and WSi_x with aided the statistical analysis of Taguchi based Grey Relational Analysis with an artificial neural network is believe the new finding in order to achieve a robust design. DG MOSFETs have captivated the attention of many researchers in recent years. Scaling the oxide thickness may result in a high tunnelling current and a decreased I_{ON}/I_{OFF} ratio, resulting in poor power consumption due to the presence of SCEs in ultra-small FETs. As a result, several innovative materials, and devices, including DG MOSFETs, have emerged as potential MOSFET alternatives. DG MOSFET design is another type of MOSFET architecture that has been used to mitigate the problems associated with the SCE [16]. When compared to planar MOSFETs, the switching action of the DG MOSFET is significantly faster. It is

widely perceived as desirable in power applications because it can be operated independently [17], [18]. The 14 nm NMOS device is virtually manufactured using the Silvaco TCAD tool and the ATHENA simulator for process simulation before using ATLAS for device simulation to obtain the device's I_D-V_{GS} and I_D-V_{DS}. According to K.E Kaharuddin et al., the fundamental benefit of a vertical double-gate MOSFET is that it has two gate electrodes that form two inversion channels, allowing it to twice the device driving current (I_{ON}) [19]. The I_{ON} of high-K dielectric materials is proportional to the permittivity of the materials. When a higher permittivity of high-K dielectrics is used as the gate insulator, it is noticed that the I_{ON} value increases. This is due to a reduction in depletion as a result from less boron absorption when a higher permittivity of high-K dielectrics is used as the gate insulator as mentioned in Ameer's experiment [20]. When developing double gate MOSFETs, it seems to be essential to keep the thickness of the silicon layers in consideration. Assure that the silicon layer thickness is low enough to allow for an overlap of the two inversion channels. Reduced drain to source penetration will prevent charge sharing effects from degrading the drive current (I_{ON}) by decreasing field penetration.

2. MATERIAL AND METHODS OF EXPERIMENT

2.1 Virtual Fabrication of n-type MOSFET using Athena Module

Due to the enormous complexity of the IC manufacturing process, semiconductor wafer fabrications (Wafer Fab) have become exceedingly expensive. Furthermore, scaling alone needs performance enhancements from one IC generation to the next, prompting chip designers to develop devices based on physics or materials that are fundamentally different from silicon [21]. To ensure that device performance continues to improve, new materials, device concepts, and optimization methodologies will be required.

In this research, the ATHENA module, a simulation tool that provided basic skills for numerical and two-dimensional simulation of semiconductor processing, is used for modelling approach. All of the virtual fabrication procedures were predicated on comparable research into High-K/Metal gate technology [7]. Using ATHENA, a double gate MOSFET with a gate length of 14 nm was practically manufactured. Following the same inherently involves transistor complementary work process, the fabrication steps are adjusted to achieve the desired result by varying a few process parameters that are within the doping density range, as forecasted by the International Technology Roadmap for Semiconductors (ITRS).

In this research, Silicon wafers oriented in the <100> and p-type (boron-doped) orientations are used as the principal substrate. $1x10^{14}$ atoms/cm^3 of boron is implanted into the silicon substrate. . It is then implanted with 20 KeV energy and 10 degrees of tilt to set the threshold voltage implant at $1.13x10^{13}$ atoms/cm^3. The 0.001 µm thick bilayer graphene is subsequently deposited. HfO_2 with a thickness of 0.002 µm is then used to deposit high-K dielectric materials to achieve the ideal threshold voltage. According to this study, the size modification of WSi_x, which operates as metal gate transistors, is scaled at 14 nm, which corresponds to the gate length of the transistor. The S/D implantation is carried out by injecting $1x10^{17}$ atoms/cm^3 of arsenic with 2 KeV energy and a 77° tilt into the p-type substrate in order to create a profoundly n-type doped region in the p-type substrate. . The 14 nm NMOS structure was then connected to aluminium metal to complete the circuit. Figures 1(a) shows the completed device for 14 nm n-type double gate MOSFET while figure 1(b) shows the measurement of the material. Due to the modification of the design of the gate, there was a difference in doping concentration. Figure 1(c) shows the doping profile of the completed device while table 1 shows a summary of the data for n-type transistor design.

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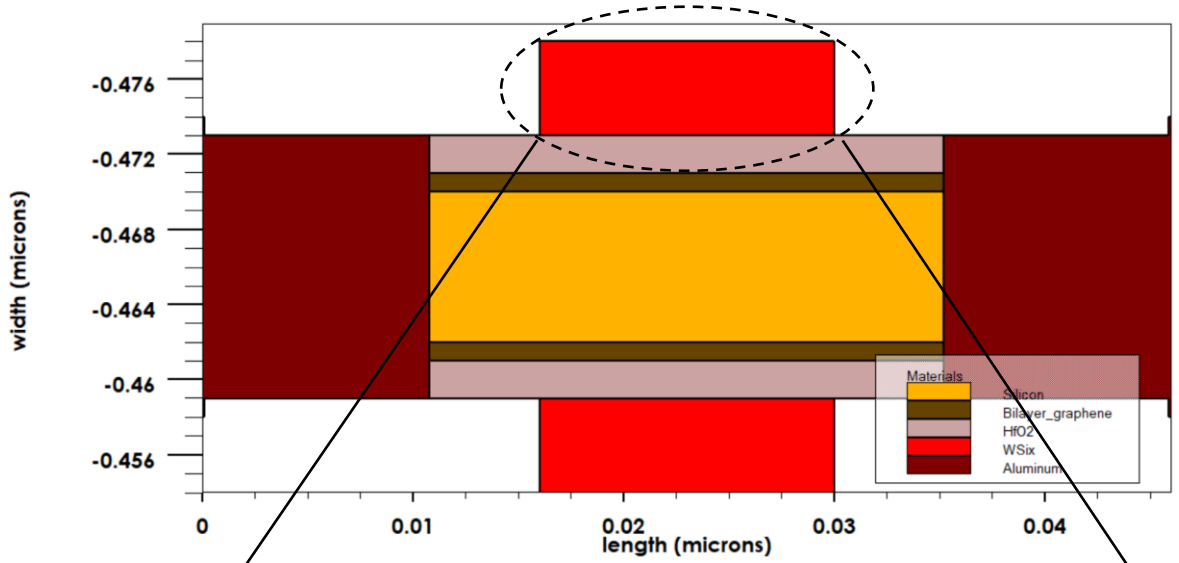

Figure 1. (a) 14nm gate length n-type device

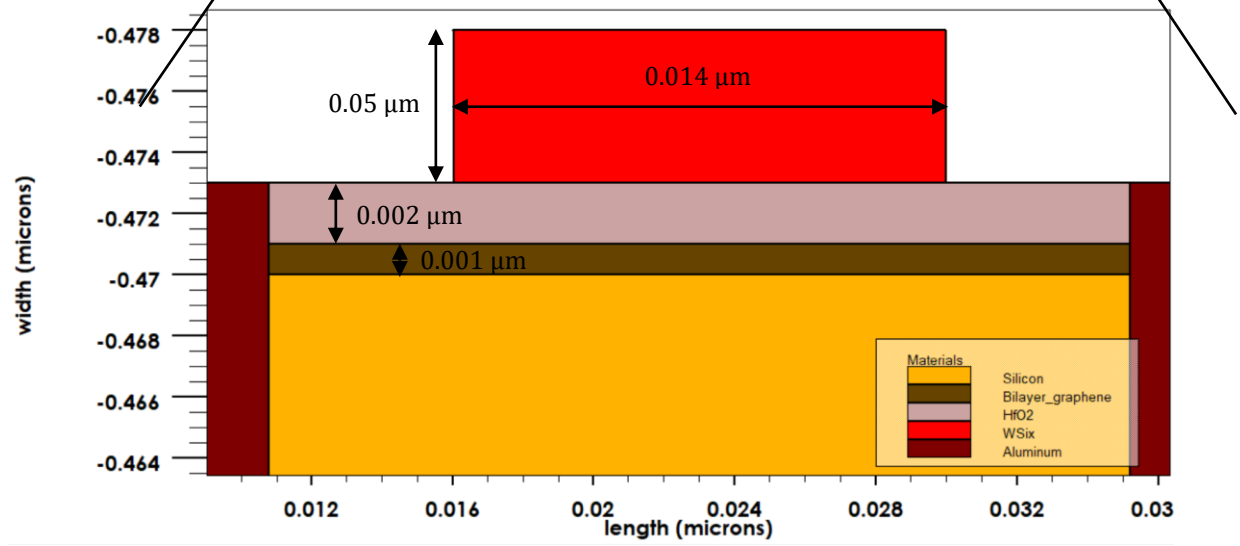

Figure 1. (b) The measurement of the material

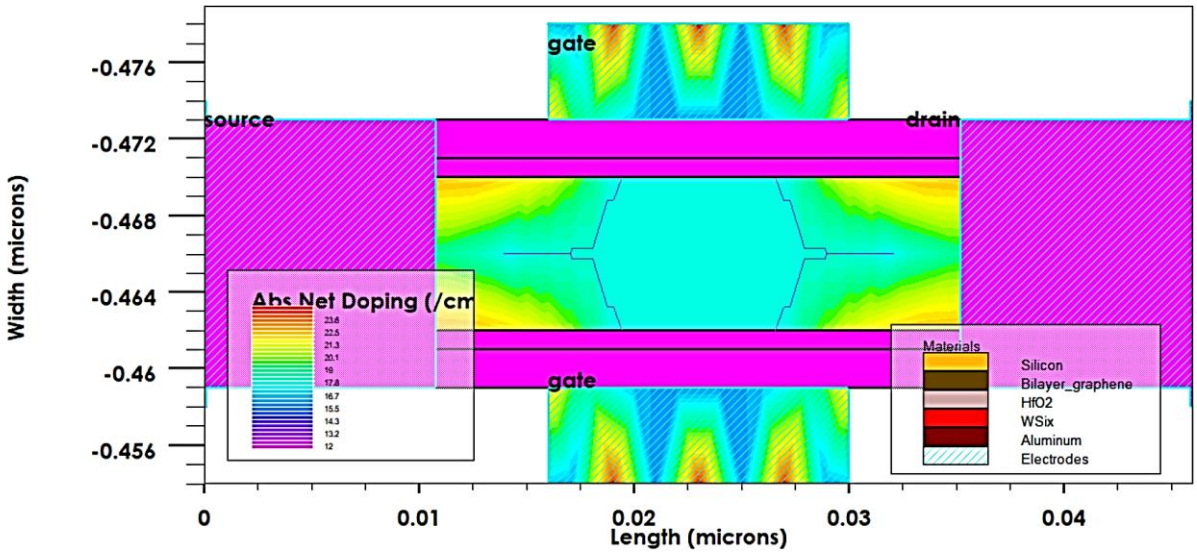

Figure 1. (c) The doping profile of the 14nm gate length n-type

Table 1 n-type MOSFET Fabrication Recipe

Process Step	n-type MOSFET parameters
Silicon Substrate	• <100> orientation
V_{TH} adjust implant	• 1.13e13cm^3 Boron • 20 KeV implant energy • 10° tilt • 30 rotations
Bilayer Graphene deposition	• 0.001 µm
High-K/metal gate deposition	• 0.002 µm HfO_2 • 0.05 µm WSi_x
Source/drain implantation	• 1e17cm^3 Arsenic • 2 KeV implant energy • 77° tilt • 60 rotations
Aluminium deposition	• 0.016 µm

The performance of the 14nm n-type MOSFET should be in line with the predictions made by the ITRS 2013 regarding the device's performance. For a specific design, there is an international standard that must be followed. Changing the dose, energy, and rotation of these implants may cause deterioration in the electrical properties of the FET device, such as the V_{TH}, I_{ON}, I_{OFF}, and SS. Statistical methods are frequently used in order to improve the overall performance of gadgets.. It is necessary to decide on all the device characteristics. In order to achieve a decreased leakage current, it is advised that the channel thickness be narrow and thin in order to allow the device to operate in depletion modes [22]. Consequently, it is essential to control process parameters like doping concentration, which have the greatest impact on the performance of a device. The idea is then put into action by developing the proposed device with the help of the TCAD programme. Doping concentration, implantation energy, and tilt angle were all parameters considered in the design of the n-type double gate MOSFET with a 14 nm channel length. Table 2 shows the summation of our input parameters.

Table 2 n-type MOSFET input parameters

Parameters	Units	Value
V_{TH} adjust implant Dose	atom/cm^3	1.13x10^{13}
V_{TH} adjust implant Energy	KeV	20
V_{TH} adjust Tilt Angle	°	10
S/D Implantation Dose	atom/cm^3	1x10^{17}
S/D Implantation Energy	KeV	2
S/D Implantation Tilt Angle	°	77

3. PERFORMANCE ANALYSIS AND RESULTS

To forecast the electrical properties of specified device structures, the ATLAS module is used. It also provides deep insight into the internal physical structure of the device that is associated with its operation. For the transistor simulation, the ATLAS module will be used to model the electrical characteristics of the transistor. Figure 2 (a) illustrates the drain current (I_{DS}) against drain voltage (V_{DS}) graph of the device at VG = 0.5 V and 1.0 V, respectively.

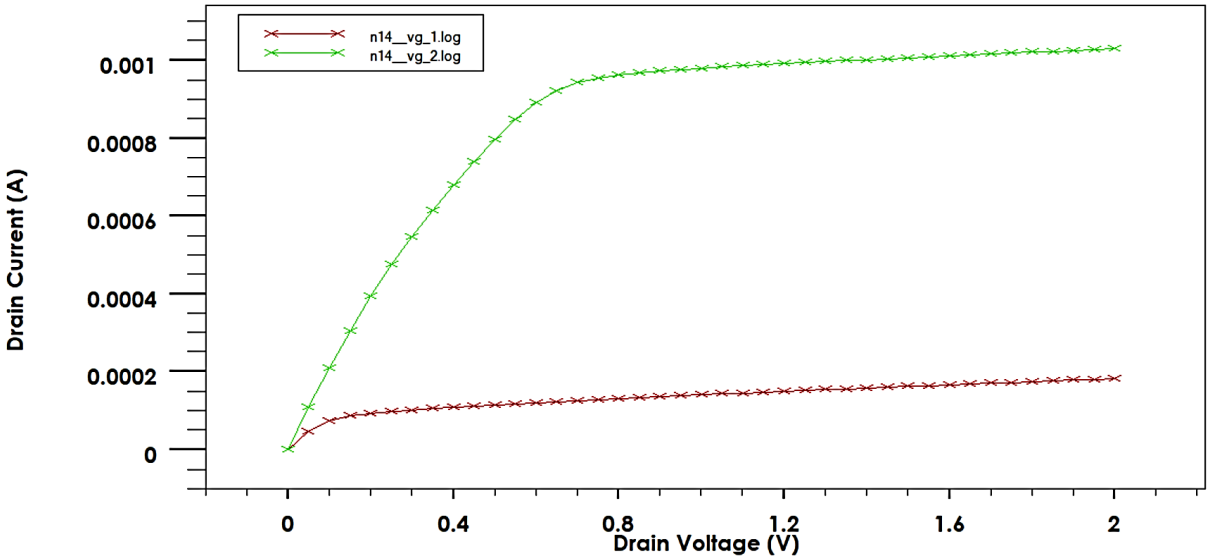

Figure 2. (a) Graph of Drain Current (I_{DS}) versus Drain Voltage (V_{DS})

Figure 2(b) represents the log file for each drain current that has been loaded, as well as the gate voltage that has been applied incrementally. As part of the simulation, the draining voltage of V_{DD} is set to 0.5 V, and the gate voltage of V_{GS} is increased by serial 0.05 V voltage steps from 0 V to 1 V during the simulation. It can be seen through the graph that V_{TH} = 0.2059 V, which is satisfactory in accordance with the ITRS 2013 forecast. Since the V_{TH} value is still within 12.7% of 0.191 V. V_{TH}, the physical dimensions of the doping channel, the surface profile, the oxide gate thickness that might influence I_{OFF}.

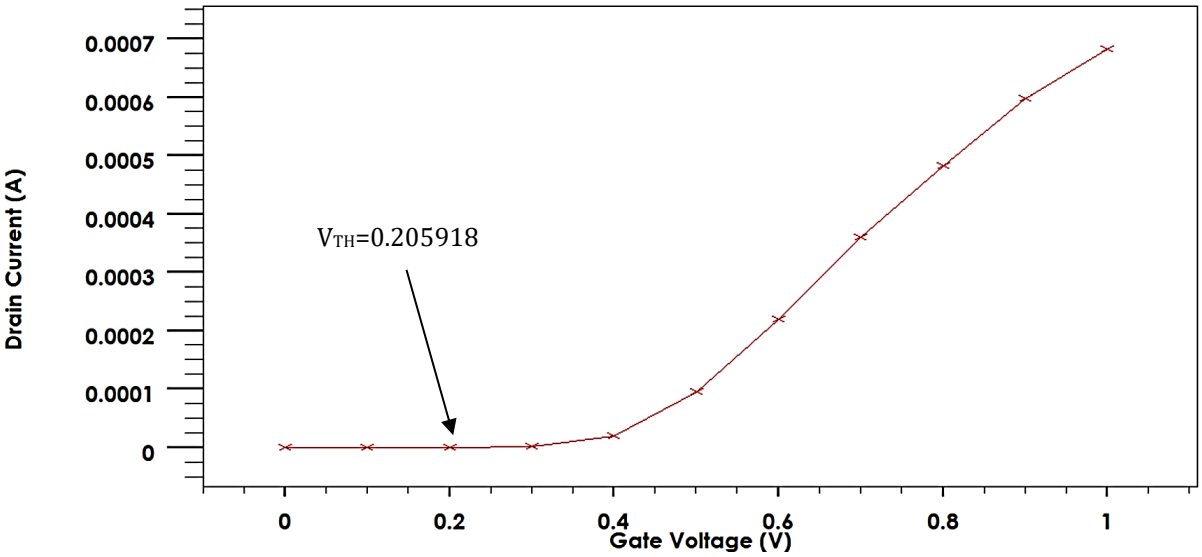

Figure 2. (b) Graph of Drain current (I_{DS}) versus Gate voltage (V_{GS})

Table 3 shows the performance parameters of the V_{TH}, I_{ON}, and I_{OFF}. The simulation results on the 14nm double gate n-type show that the simulation results of the V_{TH} and I_{OFF} are in line with what was predicted by ITRS 2013, while the value of I_{ON} is much lower than the predicted value.

Table 3 Simulation results as compared to ITRS 2013 prediction

Performance Parameter	ITRS 2013 Prediction	n-Type Transistor
V_{TH} (V)	± 0.191	0.2059
I_{ON} (μA/μm)	> 1660	797.5650
I_{OFF} (nA/μm)	< 100	29.5794

For the time being, we are concentrating on analyse the threshold voltage and leakage current to figure out the I_{ON}/I_{OFF} ratio and attain the lowest leakage current possible. Other criteria, such as Vt roll-off and DIBL to the following publication, will be considered in future works. We will also optimize both V_{TH} and I_{OFF} using Taguchi based Grey Relational Analysis with artificial neural network.

4. CONCLUSION

The simulated design of a 14nm double gate MOSFET is presented in a simple manner. The design is appropriate for the investigation of the design parameter for the purpose of performance analysis. It has been reported that the V_{TH} value is within 12.7% as predicted in ITRS 2013 which is 0.2059 V, despite the fact that the I_{ON} is lower than the projected value which is 797.5650 μA/μm the I_{OFF}, on the other hand, is attained because it is lower than 100 nA/μm, as projected in ITRS 2013 which is 29.5794 nA/μm. As a result, the device presented in this study can act as a starting point for more research and optimization to improve its overall functionality and performance. In conclusion, the entire operation of constructing a transistor with a gate length of 14 nm is both conceivable and practicable.

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