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Experimental Performance Analysis of Fabricated Si/Ge Thin Film Structure

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ABSTRACT

This paper is devoted to the evaluation of Silicon/Germanium (Si/Ge) thin film Structure based on experimental measurements. The electron beam evaporator is used to fabricate this thin film structure. The sample was prepared under high vacuum conditions (pressure of 10-5 Torr, power of 6 KV and a current of 200mA). At these conditions, it was possible to get films with thickness in the range of 300 A0. The Capacitance–Voltage (C–V) and Current–Voltage (I–V) measurements of the sample structure were performed by a staircase sweep of voltages from 0 to +5 V and back from +5 to 0 V at room temperature. The sample exhibits a low hysteresis in measurements; this hysteresis is gradually removed when the sample is exposed to a temperature until 80 °C using Carbolite Oven. Also, the sample characteristic curves of both current and capacitance are becoming smoothed instead of jagged. This sample exhibits an electroforming as a Metal Oxide Semiconductor (MOS) device over short time duration of the selected staircase double sweep, so it can be exploited as a fast-switching element in digital microelectronic circuits. In addition, the hysteresis changes over the range from room temperature until 80 °C gave light to the possibility of exploiting this sample as a proximity temperature sensor within that range of temperature.

Keywords: Capacitance –Voltage (C-V); SiGe thin films; Electron Beam Evaporator; MOS Capacitor

1. INTRODUCTION

Germanium (Ge) and Silicon (Si) have been considered as the most effective materials based electronic and optoelectronic devices. The motivating power for integration of Ge with Si attributes to its high carrier mobility, high absorption coefficient near the wavelength (1550 nm), quasi-direct band structure and relevance with Si processing technology. To date, the metal-oxide-semiconductor field effect transistor (MOSFET) is based on the application of Ge on Si [1,2], light emitting devices and some sensors have been investigated with "on-insulator" structure [3], all electronic and optoelectronic devices based on silicon and germanium integration, it is required to isolate the substrate and germanium to reduce the parasitic capacitance and leakage current [4].

Deposition of silicon over germanium technique has been used in a very wide range of applications, such as photodetectors, microelectronics, different types of photovoltaics and photonic circuits [5-6]. Beside this, there is a great interest in the complete spectrum solar cells and wide spectral optical detectors; also it is possible to provide the fabrication of Si/Ge micro or nano applications in both one dimensional and two dimensional scales due to their low thermal conductivity, high mobility of electron and

hole. In addition, they have a good compatibility with complementary metal-oxide-semiconductor which helps in extension to mid-infrared transparency [7].

Seongjae Chio, et al [8] fabricated and characterized a 1550-nm photodetector based integration of germanium over silicon coupled with silicon over silicon on insulator (SOI) platform. The effect of different metallization techniques on the responstivity characteristic has been studied. Compared to the photodetector based on a bulk metal contact, it demonstrated some improvements in the optical characteristics at low voltage operation.

Silicon over germanium has the ability to allow growing of high quality IV semiconductors group as virtual memory pixels for the silicon photonic circuits. In addition germanium layers can be used as waveguides and resonators in the fabrication of passive components. Thus, the growth of Ge on Si will be highly beneficial and cost-effective technology for the hetero epitaxial scheme. No need for ultra-high vacuum conditions to deposit the Ge on Si substrate to minimize the cost and to avoid the thermal budget effect of the deposition process [9].

The thermal budget is the balance between the absorbed heat of the sample and its radiated heat under the applied vacuum. Since the ultra-high vacuum enable short processing time and lower thermal budget, this effectively reduces the defects in the sample; consequently, a higher mobility, lower hysteresis voltage, and higher interface trap density [10]. The integration of silicon over germanium is very useful method for a wide range of applications, such as low cost III-V solar cells, on-chip photonic integrated circuits, CMOS applications and others. Most electrical and optical designs and wafer bonding technology of wide band gap applications are based on the top Si thin film [11-12].

The capacitance – voltage hysteresis of thin film structures is attributed to electron charging and discharging of the nanocrystals by direct tunneling though the ultra-thin oxide between the nanocrystals and the substrate [13-14]. The current–voltage hysteresis effects are attributed to tunneling through deep traps in the oxide. Some residuals can remain within the fabricated sample. These residuals can create intrinsic defects in the layers and unexpected charge trapping results in hysteretic behavior. Depending on the behavior of the defects, counterclockwise or clockwise hysteresis can be observed [15-17]. In this present paper, the evaluation of Si/Ge thin film structure based on experimental measurements is developed. The electron beam evaporator is used to fabricate this thin film. A double staircase bias sweep is applied across the sample with different time delays to analyze the hysteresis property of the capacitance and conductance.

2. Experimental Work

2.1 Sample Preparation

The electronic beam evaporator is used to growth the purified germanium and silicon over the glass substrate. The electric current was increased gradually through the boat to avoid breaking, when the temperature of the boat arrived to the required

temperature the deposition process starts with constant rate. After that, the power supply was turned off and the sample is left in the high vacuum. Figure 1a shows a schematic view of the obtained sample, the fabricated layers of Si or Ge or Si / Ge has top electrodes on a glass substrate. The evaporation rate was controlled through a power supply of a variable transformer (with maximum voltages of 6KV and current 500 mA) and adjusted by a thickness monitor. The distance of the substrate is 15 cm away of the evaporating boot. This process produced films having a thickness of about 300 A which were suited for electrical measurements. .During Si growth, the deposition of Ge on Si was monitored by electron-beam evaporation. Strained Si / Ge layer, have been grown on glass substrates using electron-beam evaporation deposition.

2.2 Test Equipment

Figure 1.b shows an experimental setup for measuring I-V characteristics of the sample, the I - V characteristic measurements of Ge and Si films were preformed by Agilent 4155B Semiconductor Parameters Analyzer. These measurements were taken at room temperature. The same instrument was exploited to apply a voltage across the sample and to measure the current through the films at the same time. To ensure the proper connection to the sample, the indigenously designed sample holder with aluminum electrode was used. In this arrangement the films is sandwiched between two circular electrodes from aluminum The I-V characteristics of these films have been studied using a custom built electrical switching analyzer and the current sweep.

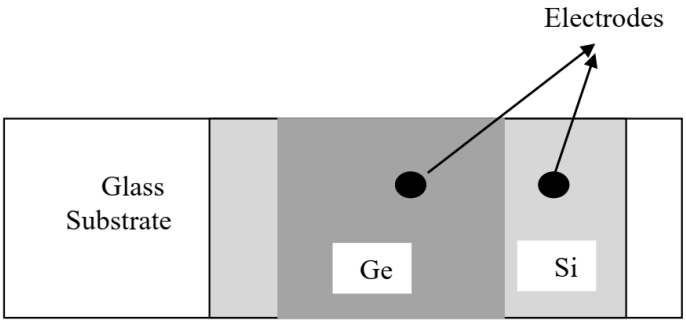

Fig. 1.a

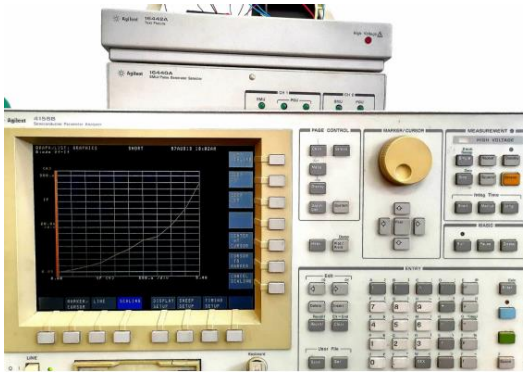

Fig. 1.b

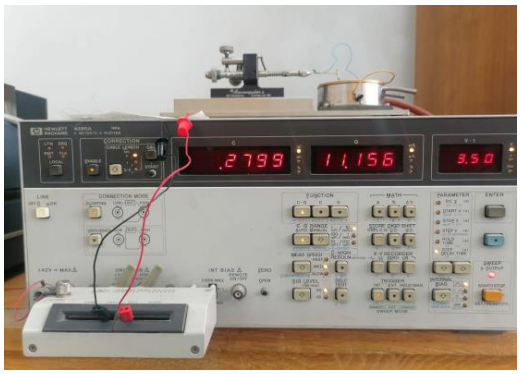

Fig. 1.c

Fig.1.a Schematic view of the prepared sample of SiGe thin film structure
Fig.1.b Experimental setup for measuring I-V characteristics of the sample
Fig.1.c Experimental setup for measuring C-V and G-V of the thin film sample

Figure 1c shows an experimental setup for measuring C-V and G-V of the thin film sample using HP C-V plotter, 4280A. The sample under test is prepared as a two terminal device and connected properly to the C-V plotter to eliminate the mutual inductance between test leads and also to reduce the effects of environmental noise. To verify best operation, an internal built in self-test signal is applied before stating measuring steps. The C-V plotter is adjusted at the C-V mode to measure the characteristics of the sample with the selected function at each step of a swept bias voltage supplied from the internal source of the instrument.

3. Results and Discussion

The measurement of capacitance-voltage is an effective method to analyze the performance of the thin film structure in terms of its dielectric and the quality of the insulator-semiconductor interface. In principle, the evaluation of capacitance against voltage can be done by moving the applied voltage over the p type from negative voltage to positive voltage which means from accumulation to inversion or over the n type from positive voltage to negative voltage which means from inversion to accumulation. The Capacitance variation of the fabricated Si/Ge thin film sample as a function of a forward applied bias voltage (C-V) ranged from 0 to +5 V at room temperature is shown in Fig. 2. As can be seen from the figure, the capacitance varies from 0 to 700 pF as the applied voltage varies from 0 to +5V. A counter clockwise hysteresis is present over the voltage range from 3.3 V to 1 V.

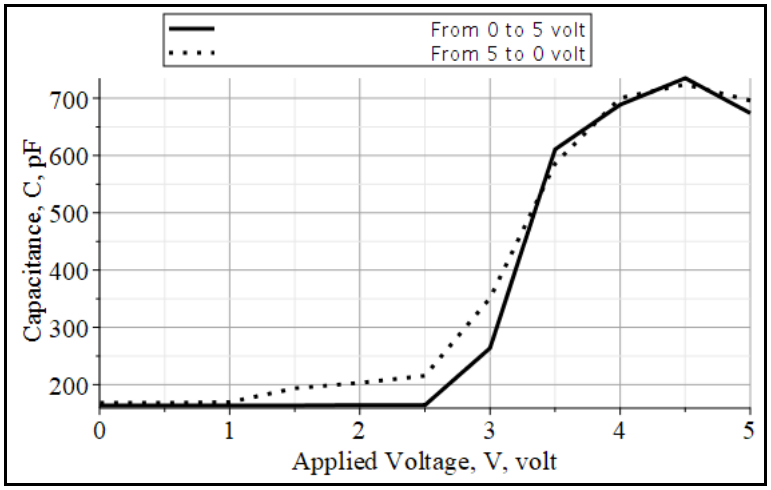

Fig. 2 Variation of capacitance against forward applied voltage at room temperature, counterclockwise hysteresis from 3.3 V to 1 V

The Capacitance variation of the fabricated Si/Ge thin film sample as a function of a reverse applied bias voltage (C-V) ranged from 0 to +5 V at room temperature is

shown in Fig. 3. Since the prepared sample may exposed to external conditions like moisture, temperature, pressure,, dust, environmental contamination, and humidity, it will exert mixing effects on its insulation characteristics, leading to equivalent parameters fluctuation and further resulting in the measurement error. The capacitance changes due to variation in electric permittivity. Also, a counter clockwise hysteresis takes place from 5 V to 2 V.

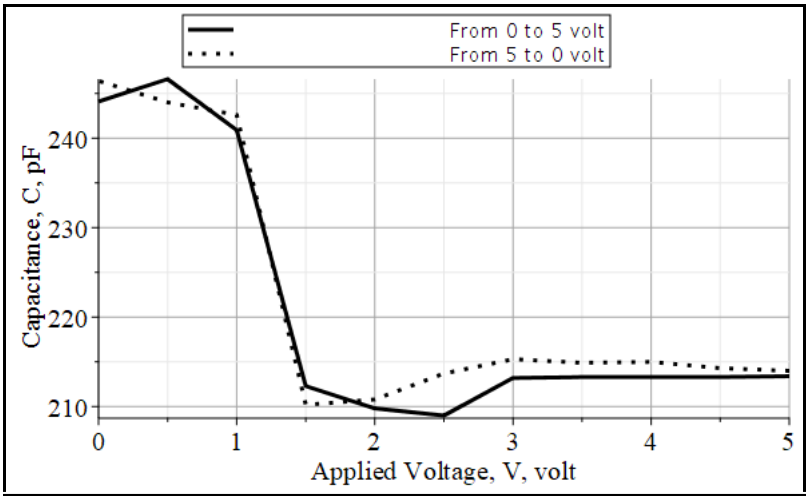

Fig. 3 Variation of capacitance against applied reverse voltage at room temperature, counterclockwise hysteresis from 5 V to 2 V

The hysteresis values of the measured capacitance or current is the maximum difference between measured output when the applied voltage approaching back from maximum to minimum. The hysteresis value is positive or negative. The positive percentage means the measured value has a higher value when the input quantity is back from maximum to minimum than the obtained value when the input quantity goes from minimum to maximum. Hysteresis in C-V measurements on thin film cells is also found by others due to the presence of deep states and the absence of Cu [18, 19]. To avoid the environmental errors resulting from the external conditions, it is required to eliminate or to reduce these undesirable errors by keeping the conditions of the experimental setup as constant as possible. The current variation of the fabricated Si/Ge thin film sample as a function of a forward applied bias voltage (I-V) ranged from 0 to +5 V at room temperature is shown in Fig. 4. As can be seen from the figure, the solid line represents the current with a nonlinear variation against the applied forward voltage and increase with the increase of it. The dotted line represents the variation of current with the applied voltage when the latter is varied from +5V to 0V. A small counter clockwise hysteresis is present from 0 V to 0.7 V, while a larger clockwise hysteresis takes place over the voltage range from 0.7 V to 5 V.

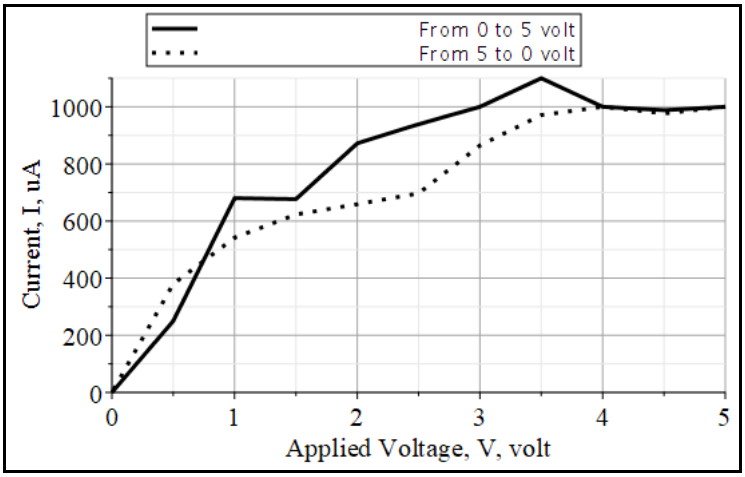

Fig. 4 Variation of current against forward applied voltage at room temperature, counterclockwise hysteresis from 0 V to 0.7 V, clockwise hysteresis from 4 V to 0.7 V

The current variation of the fabricated Si/Ge thin film sample as a function of a reverse applied bias voltage (I-V) ranged from 0 to +5 V at room temperature is shown in Fig. 5. As can be seen from the figure, the solid line represents the current with a nonlinear variation against the applied reverse voltage and increase with the increase of it. The dotted line represents the variation of current with the applied voltage when the latter is varied from +5V to 0V. A little clockwise hysteresis from 5 V to 0 V is still present over the same voltage range as exhibited in the forward connection.

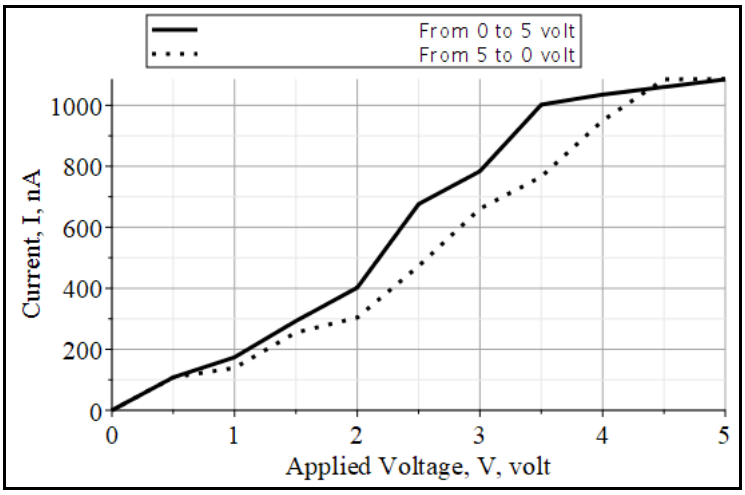

Fig. 5 Variation of Current against reverse applied voltage at room temperature, clockwise hysteresis from 5 V to 0 V

The variation of current against the applied voltage when the sample is experienced to a thermal heating of 80 °C by Carbolite Oven is shown in Fig. 6. As shown from the figure, the hysteresis of the I-V characteristics is removed by the heat. When

reversing the connection of the sample, a little change in I-V curve takes place as in Fig.7. Also, the curves become smoothed instead of jagged type. In order to improve the hysteresis that occurred in the capacitance and current measurements, the sample was inserted into an electric furnace and the temperature was gradually raised to 60 °C for 15 minutes and taken out of the oven and observed the resulting effect on the properties of the sample, where there was a somewhat improvement in the hysteresis that existed before.

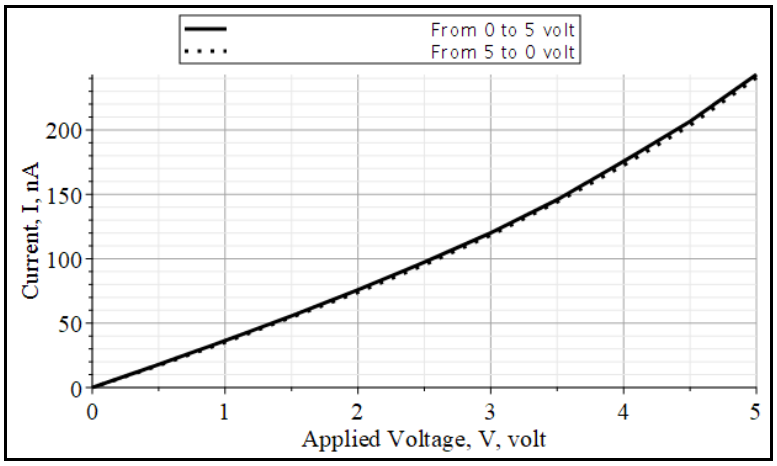

Fig. 6 Variation of current against reverse applied voltage at temperature T=80 °C, very little clockwise hysteresis from 5 V

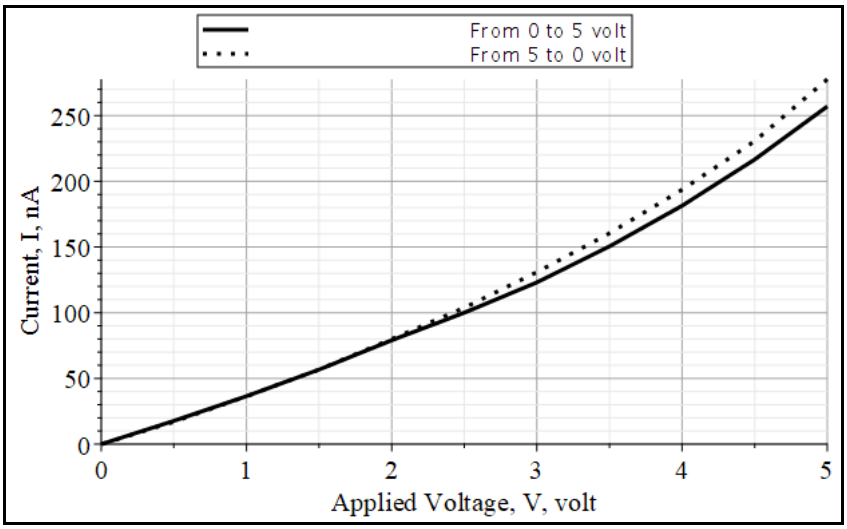

Fig. 7 Variation of current against forward applied voltage at temperature T=80 °C. little counterclockwise hysteresis from 5 V to 0 V

The sample was inserted again and the oven temperature was raised to 70 °C for another 15 minutes. Further improvement was found in the hysteresis that was present before. Then the sample was inserted again and the oven temperature was

raised to 80 °C for another 15 minutes. The improvement reached its peak at that temperature and was not affected by any increase in temperature after that as shown in Fig. 8.

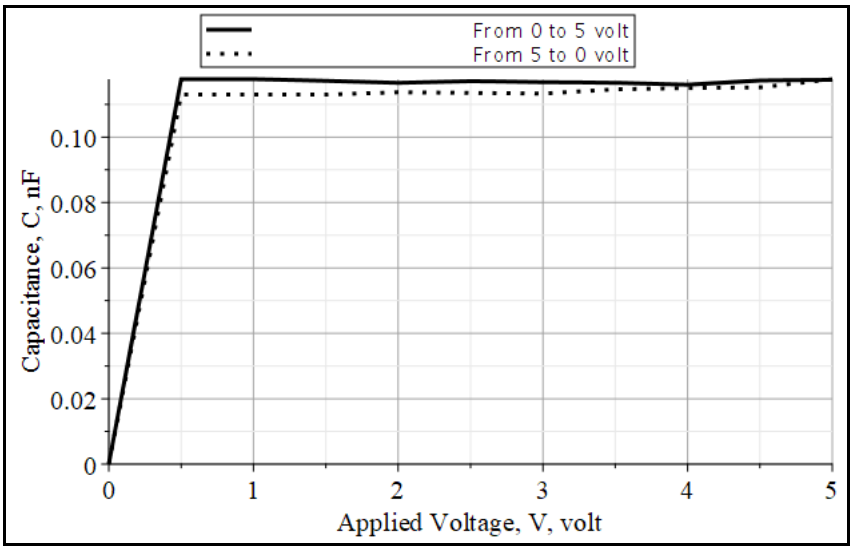

Fig. 8 Variation of capacitance against forward applied voltage at temperature T=80 °C, little clockwise hysteresis from 5 V to 0.5 V

4. Conclusions and future work

An experimental measurement analysis of fabricated Si/Ge thin film structure is developed in this article. The deposition time of the prepared sample using electronic evaporator was two hours and carried out at room temperature. The vacuum value was approximately 1×10-5 Torr. The deposition process was carried out of about 30 sec. The sample exhibits a low hysteresis for all measurements of capacitance and current over the range of applied voltage, this hysteresis was removed gradually when the sample is experienced to a temperature varied from 60 °C to 80 °C. Also the capacitance and current characteristics are became smoothed instead of jagged. Since the sample exhibits an electrical hysteresis ranging from a considerable hysteresis at room temperature to a negligible hysteresis at 80 °C, this type of sample can be exploited as a proximity sensor to ambient temperatures ranging from room temperature to 80 °C. Also, the short time duration of the selected staircase double sweep gave light to the possibility of exploiting this sample as a fast switching element for the microelectronics applications. As a future extension to this study, the electrical and optical properties of another fabricated sample of Si/Ge alloy is planned to be exploited in microelectronic devices as a fast speed device. Since this sample exhibits an electroforming mode as a MOS device, it can be exploited as a fast switching element in digital microelectronic circuits.

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