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# Impact of Dielectric Engineering on Analog/RF and Linearity Performance of Double Gate Tunnel FET

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**ABSTRACT**

Tunnel FET is one of the alternative devices for low power electronics, having steep subthreshold swing and lower leakage current than conventional MOSFET. In this research, we have implemented the idea of high -k gate dielectric on double gate Tunnel FET, DG-TFET for improvement of device features. An extensive investigation for the analog/RF and linearity feature of DG-TFET has been done here for low power circuit and system development. Several essential analog/RF and linearity parameters like transconductance($g_m$), transconductance generation factor ($g_m/I_{DS}$), its high-order derivatives ($g_{m2}$, $g_{m3}$), cut-off frequency ($f_T$), gain band width product (GBW) and transconductance generation factor ($g_m/I_{DS}$) have been investigated for low power RF applications. The $VIP_2$, $VIP_3$, $IMD_3$, $IIP_3$, distortion characteristics (HD2, HD3), 1- dB the compression point, delay and power delay product performance have also been thoroughly studied. It has been observed that the device features discussed for circuitry applications are found to be sensitive to of gate materials, design configuration and input signals.

**Keywords***:* sub threshold swing, Tunnel FET, analog, linearity, transconductance, ultra-low power

## 1. INTRODUCTION

Nowadays, low power ICs are becoming important for IoTs (internet-of-things) and portable electronics applications. The FET devices with higher $I_{ON}/I_{OFF}$ ratio and steep slope (SS) switching are essential for achieving such modern requirements. The state-of-art of Tunnel FET shows that, this device is advocated as complements of conventional MOSFETs, targeting the scaled supply voltage ($V_{DD}$<0.5V) [1-4]. Tunnel FET is a FET device uses band-to-band tunnelling (BTBT)transport operation [5-12]. The main limitation of Tunnel FET is lower on-state current ($I_{ON}$) than conventional MOSFETs [13-18]. The considerable research is to be continued worldwide to overcome the limits of on-state current, due to quantum transport mechanism. The issue of low $I_{ON}$ can be overcome by the application of low bandgap materials such as $Si_{1-x}Ge_x$ or Ge [12-15], various double gate (DG) configurations [16-21], the high-k gate dielectric, low-k spacer; III-V based hetero structure, and innovative novel architectures [7-20].

In the context of application purpose in the advancement of communication system and the high frequency devices (RF), they require minimum signal distortion in the operating region. The low power supply ($V_{DD}$), high on-current ($I_{ON}$) and subthreshold swing (SS) parameters (i.e., < 60

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mV/decade at 300 K) are not sufficient investigation for the advanced circuit and system development. The harmonic distortion (HD) arising nonlinear characteristic of the device components is an important issue for analog/RF based circuits and system design [21-24]. It is expected that, the used device components in analog/RF application should be linear. To achieve this, the high linearity, transconductance ($g_m$) should be linear over desired input voltage. However, the $g_m$ of MOSFET and Tunnel FET is variable with input voltage ($V_{GS}$) and denotes the nonlinear behaviour [8-22].

1. The linearity test of used device components can be analysed by using higher-order derivatives of $g_m$ (i.e.$g_{m2}$, $g_{m3}$), second order voltage intercept (VIP2), third order voltage intercept (VIP3) and third order intercept points (IIP3), IMD3, higher-order harmonic distortion (HD2 and HD3) and 1-dB compression point [22-32].The above discussed requirements and challenges and the needs to perform comprehensive investigative of linearity performance and distortion characteristics due to nonlinear dependency of Tunnel FET with applied input voltage. Thus, this paper will discuss these as in the following Sections.

## 2. Device Technology and Analysis Environment

In this section, a brief introduction of the device and its transfer characteristics have been investigated. The designed DG - Tunnel FET is shown in Fig.1. The present work is based on n-type configuration. Fig.1 (a) shows the 2-D cross-sectional view of designed device structures. The designed DG - Tunnel FET structure consists of source, channel configuration containing $Si_{1-x}Ge_x$ ($E_{g\text{-}SiGe} \approx 1.17 - 0.94x + 0.34x^2$) and Si ($E_{g\text{-}Si} \approx 1.12$eV) semiconductors. In the device, low bandgap materials (i.e., $Si_{1-x}Ge_x$) have kept toward source and Si toward channel region for boosting tunnelling current. The misalignment of $Si_{1-x}Ge_x$ and Si in device boosting the tunnelling current due to relatively lower tunnelling region than home channel device. For improvement of electric field inside the device, high-k gate dielectric is used instead of $SiO_2$. The designed device architectures are grouped into three possible configurations named S1, S2 and S3. In structure S1, both top and bottom gate having $HfO_2$ (k =25).In structure S2, top gate of device contains $HfO_2$ (k =25) and bottom gate contains $SiO_2$ (k=3.9). The physical dimension of $t_{ox}$ is kept 2.0 nm. Structure S3 contains $HfO_2$ (k =25) and $SiO_2$ (k =3.9) as shown in Fig.1(a). In structure S3, $SiO_2$ is staged on $HfO_2$. The physical dimensions of $HfO_2$($t_{ox1}$=1.0nm) and $SiO_2$ ($t_{ox2}$ =1.0 nm) are used. The remaining physical device dimensions and device design parameters used during investigation are tabulated in Table1.The thickness of silicon source channel has been taken as 10.0 nm, while whole channel length i.e., from source to drain region, has been taken as 50.0 nm. A uniform doping of $1.1 \times 10^{20}$ $cm^{-3}$, $5.1 \times 10^{18}$ $cm^{-3}$ and $1.1x10^{15}$ $cm^{-3}$ have been used for Source($N_s$), drain ($N_D$) and channel($N_C$) regions, respectively. The work function for gate material corresponding to this region has been set to4.6 eV.

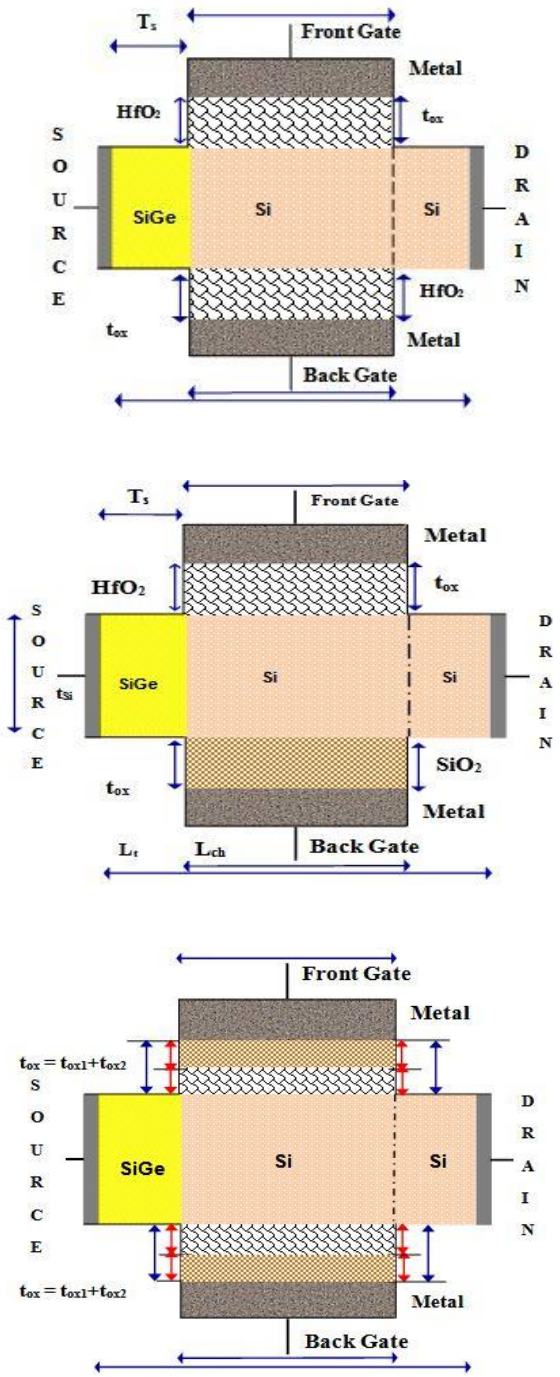



Fig.1: Proposed device structure S1, S2 and S3 Tunnel FET which includes $Si_{1-x}Ge_x$ (yellow colour) in source, Si (pink colour) in channel and drain

Table 1: Device design parameters for double gate Tunnel FET

| S.N | Symbol | Physical Parameters | Numericable value |
|---|---|---|---|
| 1 | $\phi_M$ | Work function | 4.6 (eV) |
| 2 | $N_S$ | Doping levels for source | $1.1x10^{20}$ ($cm^{-3}$) |
| 3 | $N_D$ | Doping level for Drain | $1.0x10^{18}$ ($cm^{-3}$) |
| 4 | $N_C$ | Doping level for channel | $1.1\times10^{15}$ ($cm^{-3}$) |
| 5 | $t_{ox}$ | Gate oxide material thickness | 2.0 (nm) |
| 6 | $L_t$ | Total length of the device | 250.0 (nm) |
| 7 | $L_{ch}$ | Channel length | 50.0 (nm) |
| 8 | $t_{Si}$ | Silicon film thickness | 10.0 (nm) |
| 9 | $L_S/L_D$ | Source and drain lengths | 100.0 (nm) |

All reported results in this research have been carried out using Silvaco/ATLAS device simulator version 3.1.20.1.R. The mesh size is$5x10^{-4}$µm at interface source/channel. To obtain the best convergence and a low computation time, the Newton's numerical method based on iteration has been chosen. All investigations are based on 40.0% Ge content in $Si_{1-x}Ge_x$. The nonlocal BTBT model has to be accompanied by a fine quantum meshing around the expected tunnelling area. To calibrate the OFF current, the SRH (Shockley Read Hall) recombination models has been be incorporated as the BTBT model. To specifies that the standard concentration dependent mobility, parallel field mobility, Shockley-Read-Hall recombination with fixed carrier lifetimes, Fermi Dirac statistics and Silberberg impact ionization models have been used.

## 3. RESULTS AND DISCUSSION

### 3.1 DC Characteristics

The DC characteristic of device architectures, S1, S2 and S3 shown in Fig.1 is presented in this section. Fig.2 and Fig.3 show the typical transfer ($I_{DS}$ -$V_{GS}$) and $g_m$ -$V_{GS}$ characteristics for device architectures S1, S2 and S3 shown in Fig.1. It has been observed that the structure S1(i.e., Fig.1 (S1))shows the best device design matrix elements in term of $V_{th}$ ( $\approx$ 0.38V) and average-SS ( $\approx$ 28.19 mV/decade)calculated by Equation (1) has been obtained. The on-state current ($I_{DS} \approx 10^{-3}$A/µm) and off-state current ($I_{OFF} \approx 10^{-17}$ A/µm) are measured during simulation. It has been noticed that, the use of symmetric gate dielectric (shown in Fig.1 (S1)) creates optimum performance. Other two configurations containing composite dielectric gate materials do not causes significant improvement in electrostatic performance. The dependency of transconductance ($g_m$) over applied $V_{GS}$ shows the nonlinear behaviour like conventional MOSFETs [22-30]. The extracted electrical parameters of the devices are shown in Table2. During investigation, it has been observed that there is a shift of the maximum $I_{ON}$ of one decade and shift of threshold voltage is ~ 0.22 V between designed structure S1, S2 and S3. As shown in Fig.2, point subthreshold of structure S1 is smaller than other structure S2 and

S3, pointed as $SS_{Point-1}$ and $SS_{Point-2}$ and $SS_{Point-3}$. The $I_{ON}/I_{OFF}$ ratio of structure 1 is larger than other configurations.

As shown in Fig.2, for supply voltage, $V_{DS}$ = 0.5V, the steep sub threshold characteristics (SSpoint) is improving in case of structures S1 containing high-k, $HfO_2$ in front and back gate. The off state switching current is almost same, order of ~ $10^{-17}$A/μm. In structure S1, $I_{ON}$ ~ $10^{-3}$A/μm. The $g_m$ changes with the change in $I_{DS}$ with respect to $V_{GS}$ for fixed voltage at the drain voltage $V_{DS}$ = 0.5 V is shown in Fig. 3. It has been noticed that the $g_m$ increases with increased value of $V_{GS}$ and for higher $V_{GS}$ and the $g_m$ reaches its peak and begins to falling. The fall of peak in $g_m$ at particular input voltage shown no linearity and limits of high frequency applications. The average subthreshold slope of designed structures, shown in Table 2, is calculated by Equation (1) [1, 29] respectively.

$$SS_{Average} = {}^{V_{DD}}/_{\log 10\left({}^{I_{ON}}/_{I_{OFF}}\right)} \quad (1)$$

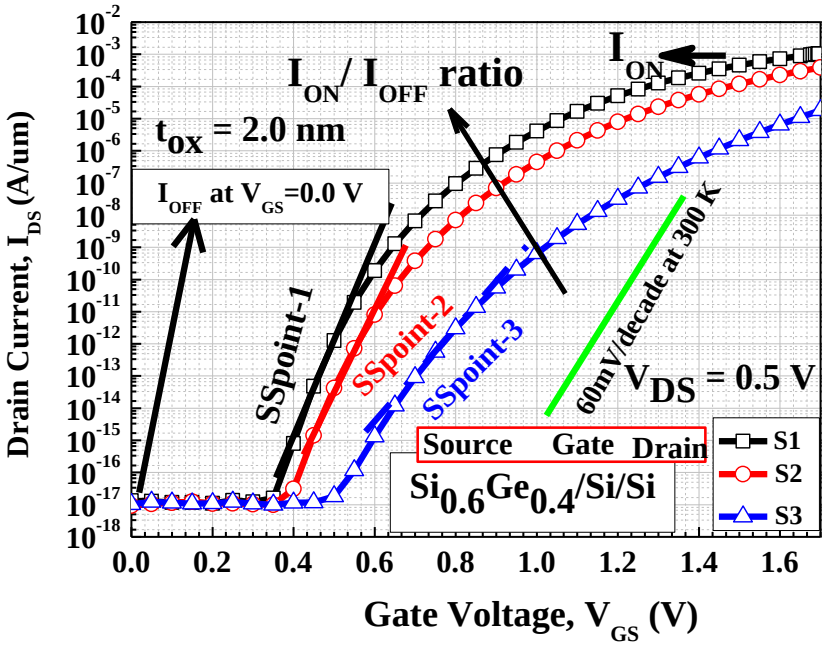



Fig.2: Typical $I_{DS}$ versus $V_{GS}$ characteristics of designed DG - Tunnel FET structures

The transconductance $g_m$ of Tunnel FET depends on the nature of $I_{DS}$-$V_{GS}$ and is shown by Equation (2) [25-28]. It has been observed that, there is an improvement in $g_m$ with homo dielectric gate material (i.e., S1) with $V_{GS}$, which is due to the improvement electrostatic due to high-k, $HfO_2$(k ≈ 25). A clear peak of $g_m$ versus $V_{GS}$ is noticed in Fig.2. For symmetric high-k, staggered DG -TFET (i.e., S1), there is a clear difference in the magnitude of $g_m$-max (i.e., clear separation of $g_m$ - max). Fig. 3 shows the optimum $g_m$-max (≈ 3.31×$10^{-3}$ S/μm).

Table 2: Summary of collected device design parameters of Tunnel FET Device

| S.N. | Structures | $I_{ON}$ (A/µm) | $I_{OFF}$ (A/µm) | $I_{ON}/I_{OFF}$ ratio | $V_{th}$ (V) | $SS_{Average}$ (mV/dec) |
|---|---|---|---|---|---|---|
| **S1** | FG: $HfO_2$<br>BG: $HfO_2$ | $1.03\times10^{-3}$ | $1.31\times10^{-17}$ | $0.79\times10^{14}$ | 0.38 | 28.19 |
| **S2** | FG: $HfO_2$<br>BG: $SiO_2$ | $9.88\times10^{-5}$ | $1.31\times10^{-17}$ | $7.54\times10^{12}$ | 0.56 | 30.17 |
| **S3** | FG: $HfO_2$/ $SiO_2$<br>BG: $HfO_2$/ $SiO_2$ | $1.80\times10^{-5}$ | $1.31\times10^{-17}$ | $1.37\times10^{12}$ | 0.82 | 47.82 |

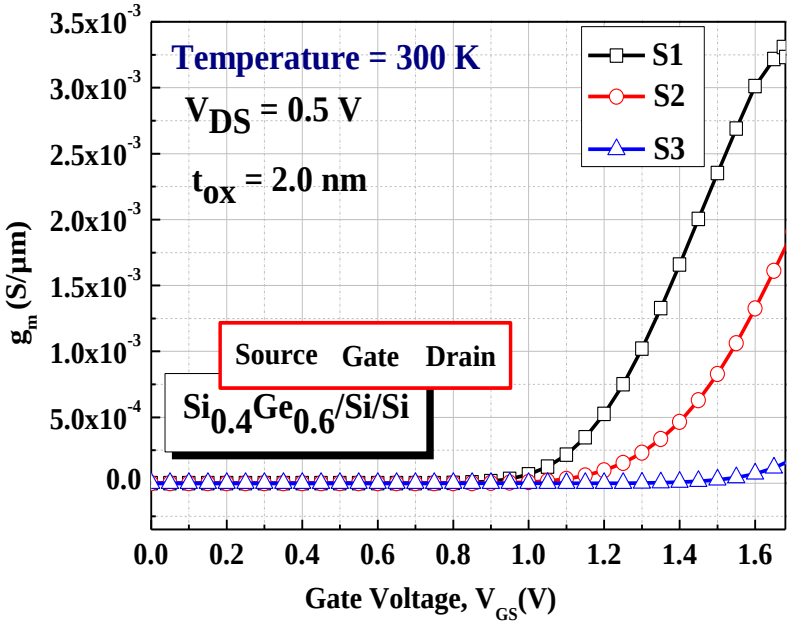



Fig.3:$g_m$ versus $V_{GS}$ characteristics of designed DG - Tunnel FET structures

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} (2)$$

Fig. 4 shows the qualitative analysis of design Tunnel FET structures in term of Vth and $I_{ON}$. This figure strongly recommends that structures S1 have superior characters in term of $I_{on}$ and $V_{th}$. The structure S1 is having smallest value of $V_{th}$ and a larger $I_{on}$ current.

### 3.2 Analog/RF Figure of Merits

The transconductance, $g_m$ is not only an essential circuit design element for analog/RF applications based circuit and system but also important in choosing an optimum bias point [22-30]. The analog/RF, figure of merits (FoMs) has been observed in terms of $g_m$, cut off frequency ($f_T$) and gain band width product (GBW). As per analog/RF application, ideally it is expected that $g_m$ should be linear for applied voltage range. Practically, both FET devices, MOSFETs and Tunnel FETs show nonlinearity.

The linearity test of design TFET structure ensures the variation of device characteristics for applied input voltage, $V_{GS}$ range in high frequency applications. The optimized linearity of circuit design for analog/RF application is basic requirements for analog/RF design. The following section has dedicated to C-V analysis of structure S1, S2 and S3. For C-V analysis, AC simulation is performed by coupling an input small signal with DC bias at the gate terminal. The C -V characteristic of n-channel DG -Tunnel FET is shown in Fig. 5. This figure shows the capacitance(C) variation versus applied ($V_{GS}$) and quantities comparison of designed structure (S1, S2 and S3). It also shows the variation of gate capacitance versus applied input gate voltage. It indicates an increase in the capacitance(C) from bottom to top at the threshold voltage. The Gate-Gate capacitance (Cgg) is mainly composed of two capacitances, Gate-Drain (Cgd) and Gate-Source (Cgs). It is known that, Gate-Source capacitance (Cgs) is lower because of the presence of the tunnel effect while the Gate-Drain capacitance (Cgd) is a dominant capacitance due to the accumulation of the electrons of the Channel-Source and collected by the drain region.

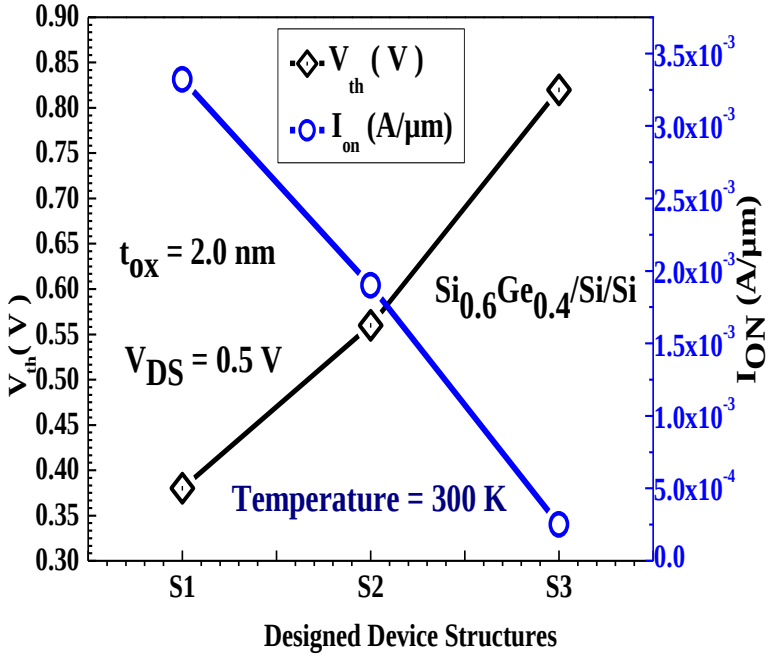



Fig. 4: Typical $V_{th}$ and $I_{on}$ characteristics of designed DG - Tunnel FET structures, S1, S2 and S3

Fig.5 advocates the importance of high - k materials and replacement of the $SiO_2$ (k = 3.9). As shown here, gate capacitance is sensitive with applied input voltage, $V_{GS}$. The $C_{gg}$ is varying in $V_{GS}$. The gate with high - k material, allowing the capacitance of the gate to be increased without the leakage effects. The cut-off frequency ($f_T$) is used to evaluate the frequency characteristics of electronic devices, and can be obtained by the ratio of $g_m$ over Cgg, following Equation (3). Fig. 6 plots comparison of $f_T$ with $V_{GS}$ for different devices structure S1, S2 and S3. It is clear from here that S1 has optimum $f_T$, however variation with $V_{GS}$ is similar in all three structure S1, S2 and S3.

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} = \frac{g_m}{2\pi C_{gg}} \qquad (3)$$

In Fig. 6, as the gate voltage ($V_{GS}$) increases, the cut-off frequency ($f_T$) increases following Equation (3) to reach its maximum ($f_{T\text{- max}}$), then increasing Cgg, start goes down, as soon as the gate voltage exceeds the threshold voltage. The $f_T$ varies slightly lager in S1 with $V_{DS}$ = 0.5 V. This is due to the on-state current ($I_{DS}$) and its $g_m$ value. These designed parameters are strongly depending on band-to-band tunnelling of charge carriers controlled by applied electric field.

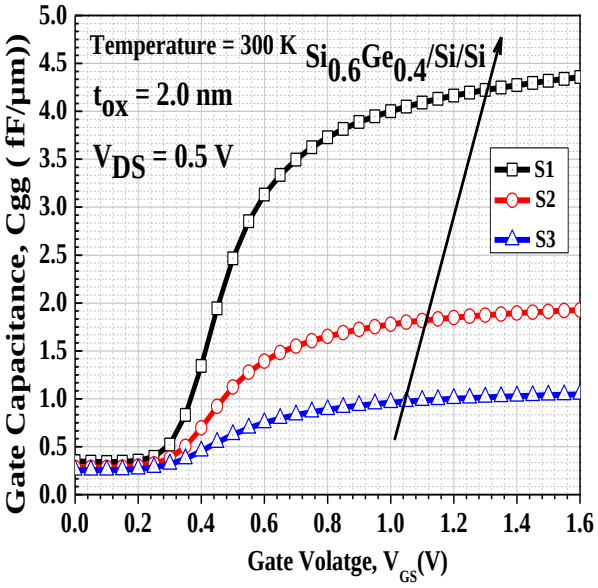



Fig.5:C-V characteristics of the designed DG- Tunnel FET structures. The arrow indicates the Cgg is increasing with $V_{GS}$ and S1 has larger Cgg than S2 and S3

$$GBW = \frac{g_m}{2\pi\ 10\ C_{gd}} (4)$$

It has been noticed that, the gain bandwidth (GBW) product, an important design parameter, the analysis of frequency response, can be calculated by the Equation (4) is investigated in Fig.7. Fig.7shows the impact of applied $V_{GS}$ on GBW product. Fig. 7 indicates that, GBW increases with the increased $V_{GS}$ until it reaches a maximum and then decreases as soon as $V_{GS}$ is close to the low voltage of the Tunnel FET device. The similar variation for the cut-off frequency ($f_T$) versus $V_{GS}$ has been obtained. In case of low-k/high-k mixed configuration, difference between two $g_m$ peaks reduced, resulting lower $\boldsymbol{f}_T$ and GBW.

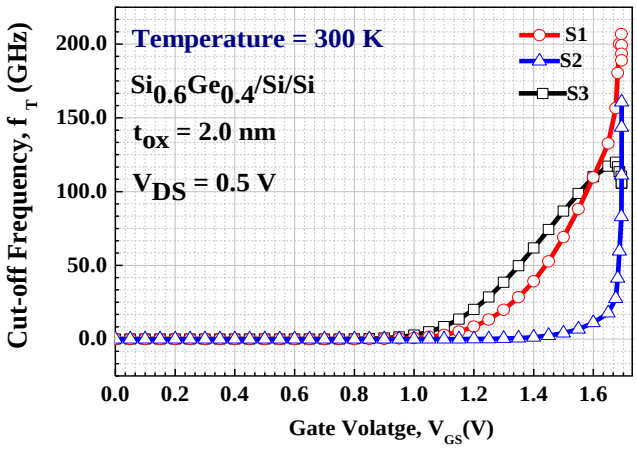



Fig. 6: Cut-off frequency variation with respect to $V_{GS}$

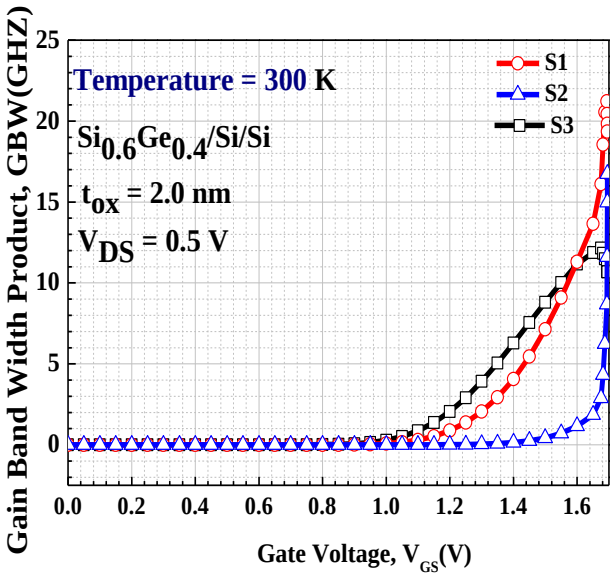



Fig. 7: Gain bandwidth (GBW) product variation with respect to $V_{GS}$

Structure S1 shows the optimum $g_m$ than other structure S2 and S3, shown in Fig.2, while $C_{gg}$ is also optimum at same device design parameters and operating condition, shown in Fig.5. This cause intermediate value of $\boldsymbol{f}_T$-max (≈206.70 GHz) and $GBW_{max}$ (≈21.22 GHz), as resumed in Table2. The obtained $g_{m\,-}$ max, $\boldsymbol{f}_T$-max and $GBW_{max}$ of designed TFET structure is summarised in Table2. This can be understood by investigating Equation (3) and (4). While in case of S1, $|C_{gg}|$ is larger than other structure S2 and S3, simply followed by $C = \epsilon_r \left(A/d\right)$, this causes intermediate value of $\boldsymbol{f}_T$-max and

$GBW_{max}$, shown in Table2. While $|C_{gg}| > |C_{gd}|$ cause lower value of $GBW_{max}$ than max, as shown in Fig. 7 and Table 3. This is formulated with the help of Equations (5), (6) and (7).

The histograms in Fig. 8 shows clearly a peak of structure homo high- k that $\boldsymbol{f}_T$ achieve 200 GHz and average-SS is very low that confirm least energy consummation and the bandwidth of transistor is greater than to the other two structures.

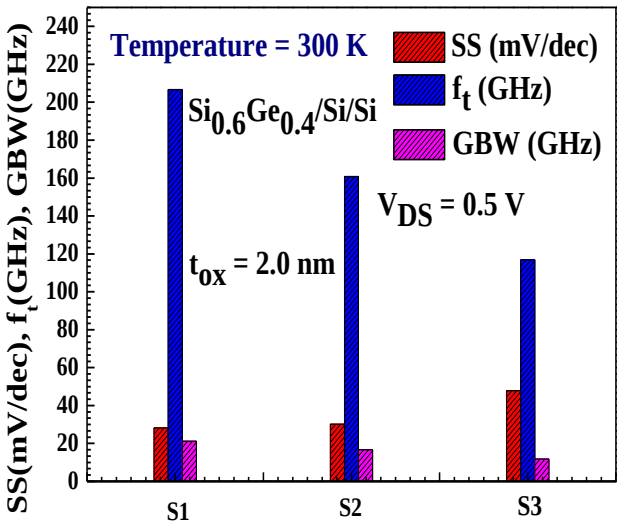



Fig. 8: Histogram for SS, $f_T$ and GBW designed DG - Tunnel FET structures

The key parameters of amplification are transconductance generation factor, TGF ($g_m/I_{DS}$) following Equation (8) is shown in Fig.9. The plot of TGF (i.e. $g_m/I_{DS}$) versus input voltage $V_{GS}$ is shown in Fig.9. The$g_m/I_{DS}$ factor is weaker dependency with applied voltage. The peak $g_m/I_{DS}$ has obtained around 0.4 V of maximum value 600 $V^{-1}$. The clear peak of TGF for S1 shows the optimum value. Its maximum value $(g_m/I_{DS})_{MAX}$ is obtained when the $V_{GS}$ is close to $V_{th}$ the captured $(g_m/I_{DS})_{MAX}$ values for device structure S1, S2 and S3 as shown in Table4. The higher value of TGF indicates smooth operation of the analog circuit even for low power supply, indicate designed device structure S1 (≈ $600V^{-1}$) is better choice for low power circuit and system.

$$y_{f\,T} = f(g_m, C_{gg}) \qquad (5)$$

$$y_{GBW} = f(g_m, C_{gd}) \qquad (6)$$

If $|C_{gg}| = |C_{gd}|$, then

$$|y_{fT}| = |y_{GBW}| = f(g_m, C_{gg}) \qquad (7)$$

Table3: Extracted device parameters for analog/RF applications

| S.N. | Structures | $(g_m)_{Max}$ (S/μm) | $f_{max}$ (GHz) | $GBW_{Max}$ (GHz) |
|---|---|---|---|---|
| **S1** | FG: $HfO_2$<br>BG: $HfO_2$ | $3.32\times10^{-3}$ | 206.70 | 21.22 |
| **S2** | FG: $HfO_2$<br>BG: $SiO_2$ | $1.90\times10^{-3}$ | 160.80 | 16.73 |
| **S3** | FG: $HfO_2$/ $SiO_2$<br>BG: $HfO_2$/ $SiO_2$ | $2.50\times10^{-4}$ | 116.80 | 11.83 |
| Note: FG, BG stands for front and back gate. | | | | |

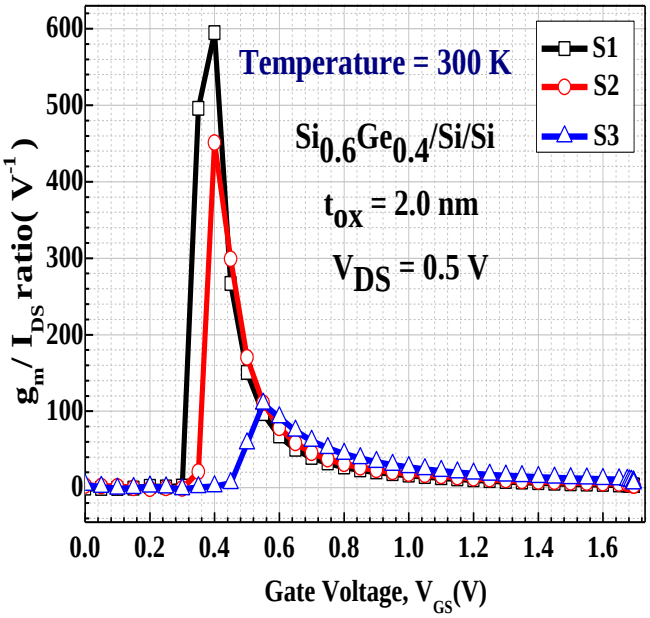



Fig. 9: Variation of $g_m/I_{DS}$ ratio with $V_{GS}$

$$\left.\frac{g_m}{I_{DS}}\right|_{Max} = \lim_{V_{GS}\to V_{OFF}} \left(\frac{g_m}{I_{DS}}\right) (8)$$

Table 4: Extracted device parameters maximum of $g_m/I_{DS}$

| S.N. | Structures | $(g_m/ I_{DS)\text{-}Max}$ $(V^{-1})$ |
|---|---|---|
| **S1** | FG: $HfO_2$<br>BG: $HfO_2$ | 600 |
| **S2** | FG: $HfO_2$<br>BG: $SiO_2$ | 450 |
| **S3** | FG: $HfO_2$/ $SiO_2$<br>BG: $HfO_2$/ $SiO_2$ | 100 |

### 3.3 Investigation of Linearity Performance

In modern low power electronic system design requirements, high $I_{ON}$, low SS and low off- current ($I_{OFF}$) are not the sufficient required FoMs by which to analyse device performance. Linearity is an additional important parameter for device qualification, which is known for its use in analog circuits. In linearity, output is related to input. In this section, the linearity performance investigation of designed device architectures, S1, S2 and S3, shown in Fig.1 is presented. Due to various gate dielectric topologies, these devices show dissimilar electric field inside tunnelling junction. The designed device structures have been simulated to carry out the linearity performance.

The nonlinear behaviour of Tunnel FET with $V_{GS}$ is cause of harmonics in the device. Though there is infinite number of harmonics, only first three harmonics i.e.,$g_{m1}$, $g_{m2}$ and $g_{m3}$ concise the effect. For the use of RF applications, the device should be fewer harmonic distortions and more linear with applied voltage range. The linearity behaviour of designed device structure, shown in Fig.1(S1, S2 and S3) is verified by analysing certain parameters such as C-V characteristics, higher order derivatives of $g_m$ (i.e., $g_{m2}$ and $g_{m3}$), high order harmonic distortions (HD2, HD3), IIP3, IMD3, second order voltage intercept (VIP2) and third-order voltage intercept point (VIP3)[22-30].

In the following analysis of linearity for devices, $g_{m1}$, $g_{m2}$ and $g_{m3}$ are expressed by Equation (9) and (10). The $g_m$ and its higher order derivative characteristics cause harmonic distortion in FET devices. The $g_{m3}$ determines the lower limits on the distortion, and hence, the amplitude of $g_{m3}$ should be low.Fig.10 shows the variation of $g_{m2}$ and$g_{m3}$ with $V_{GS}$at supply voltage, $V_{DS}$= 0.5 V. From this figure, we concluded that, the higher order derivative of $g_m$ for the device structure S1 is optimized than any other Tunnel FET configuration S2 and S3. The peak of $g_{m3}$ indicates lower limit of nonlinearity.

The second order voltage intercept ($VIP_2$) is a FoMs which determines the distortion characteristics for different dc parameters. For high linearity performance and low distortion operation, a high value of $VIP_2$ is required [23-30]. The $VIP_2$and third order voltage intercept ($VIP_3$) represent the extrapolated gate-voltage amplitudes at which the second- and third-order harmonics, respectively, become equal to the fundamental tone in the device drain current ($I_{DS}$). These are the suitable FoMs, which can properly determine, the distortion characteristics from DC parameters to achieve high

linearity and low distortion operations. These linear test design matrix elements should be as high as possible. The $VIP_2$ and $VIP_3$ follow the following Equation (11) and (12) [25-26]. The $VIP_3$ peak, shown in Fig.11 for design device S1reflects the cancelation of the third order non-linearity coefficient by the device and the internal feedback around the second-order non-linearity.

$$g_{mn} = \frac{1}{n!}\left(\frac{\partial^n I_{Ds}}{\partial V_{gs}^n}\right), \ \ where\ n = 1,2,3 \qquad (9)$$

$$\begin{cases} g_{m1} = \left[\dfrac{\partial I_{DS}}{\partial V_{GS}}\right]_{V_{DS=Constant}} \\ g_{m2} = \left[\dfrac{\partial^2 I_{DS}}{\partial V_{GS}^2}\right]_{V_{DS=Constant}} \\ g_{m3} = \left[\dfrac{\partial^3 I_{DS}}{\partial V_{GS}^3}\right]_{V_{DS=Constant}} \end{cases} \qquad (10)$$

The third third-order intermodulation distortion ($IMD_{3)}$ determines the distortion performance of a device, which should be low for minimization of distortion and is given by Equation (13) [25-26]. The IMD3, FoMs representing the extrapolated intermediation power at which the first-and third-order intermodulation powers are equal.Fig. 12 shows the IMD3 as a function of $V_{GS}$ in the logarithmic scale (unit: decibels) for device structure S1, S2 and S3 for $V_{DS}$ = 0.5 V. From this figure, we observe that the amplitude of the IMD3 signal of S1 is weak. This means that the power distortion is as low as possible, which confirms better device linearity.The third-order intercept point (IIP3) is another FoMs which evaluates the linearity performance and is given by Equation(14) [25-26]. The IIP3 is the power to which the power of 1st and 3rd harmonics is equal. It should be as high as possible to maintain linearity. From the simulation results presented in Fig. 13, it shows that the structure S1 presents a peak of IIP3 the highest. The $R_S$ = 50Ω [23] is taken for IIP3 estimation of device.

$$VIP_2 = \left[\sqrt{4\left(\frac{g_{m1}}{g_{m2}}\right)}\right]_{V_{DS=Constant}} \qquad (11)$$

$$VIP_3 = \left[\sqrt{24\left(\frac{g_{m1}}{g_{m3}}\right)}\right]_{V_{DS=Constant}} \qquad (12)$$

$$IMD_3 = R_S[4.5.(VIP_3)^3.g_{m3}]^2 \qquad (13)$$

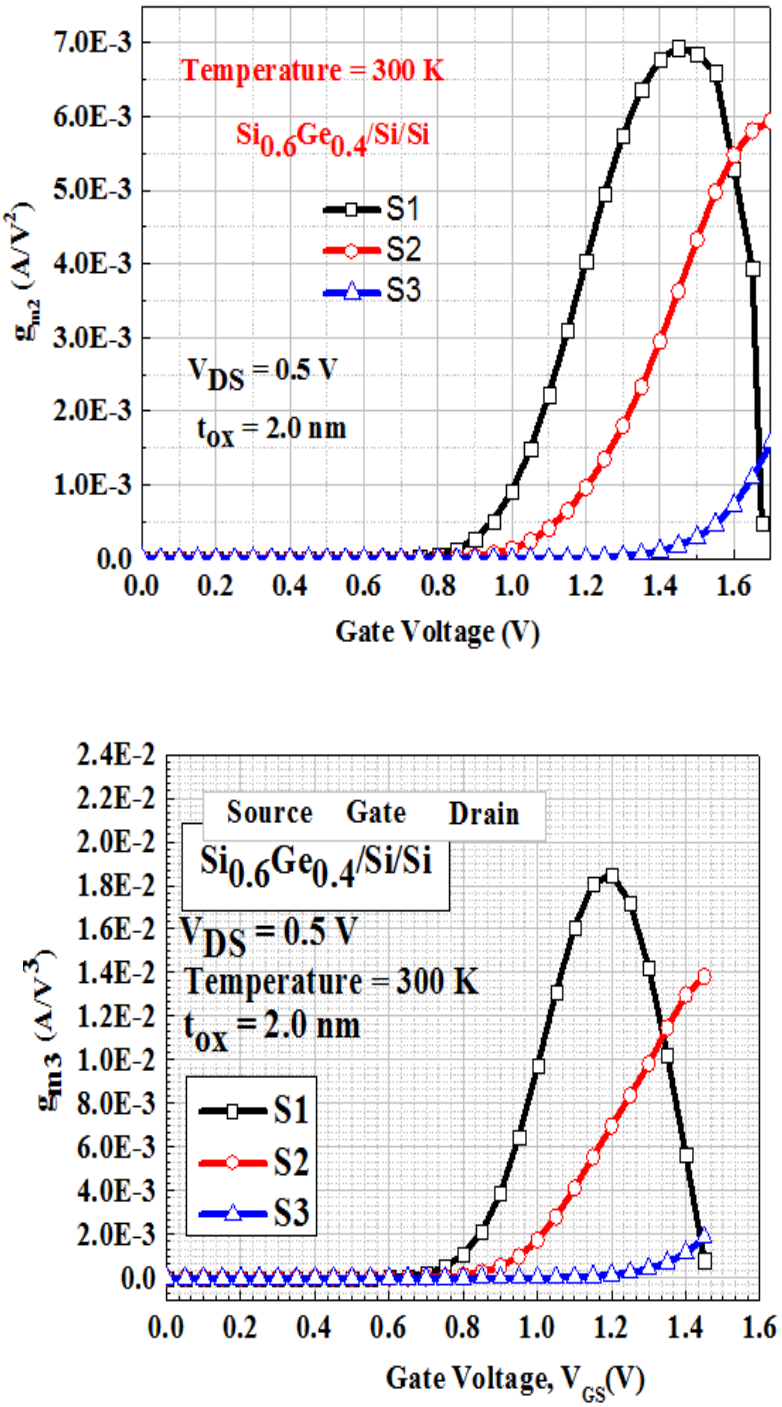
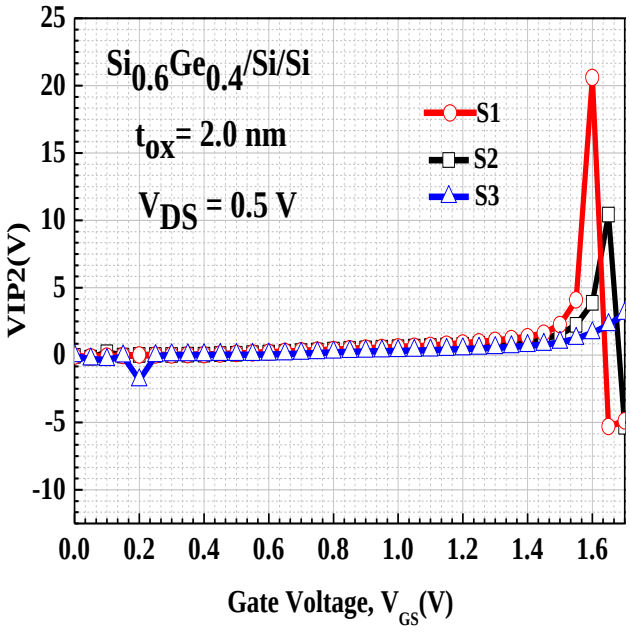



Fig.10: Variation of $g_{m2}$ and $g_{m3}$ with applied $V_{GS}$



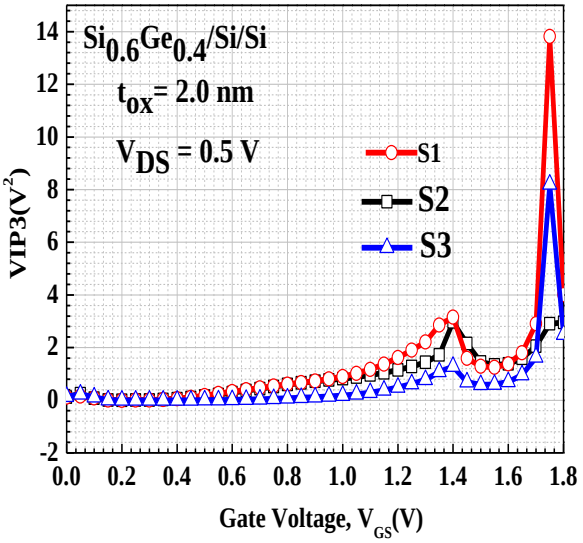




Fig. 11: Variation ofVIP2 and VIP3 with applied $V_{GS}$

The 1- dB compression point is considered as a reliable measure of linearity evaluation at the onset of distortion and is given by Equation (15) [25-27]. The 1- dB compression point indicates the power level that causes the gain to drop by 1- dB from its small signal value. Fig. 14 shows the compression

point of 1- dB of all the structures studied in this work. It is clear that the proposed S1 structure has a higher value of the compression point of 1- dB.

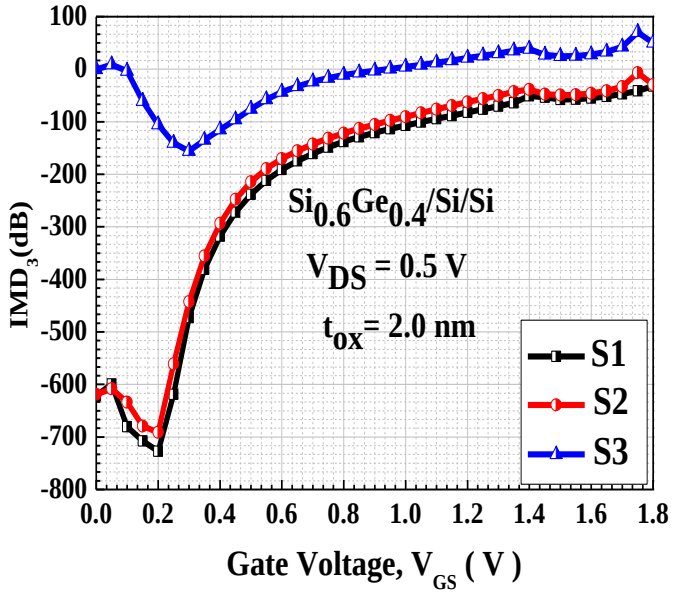



Fig.12: IMD3 variation with respect to $V_{GS}$

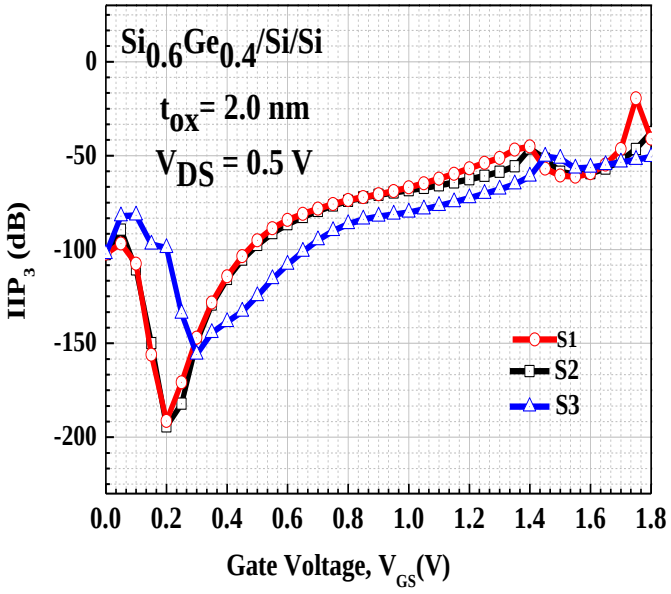



Fig. 13: IIP3 variation with respect to $V_{GS}$

$$IIP_3 = \frac{2}{3}.\frac{g_{m1}}{g_{m3} \times R_S} \quad (14)$$

$$\text{1-dB compression point} = 0.22\sqrt{\left(\frac{g_{m1}}{g_{m3}}\right)} \quad (15)$$

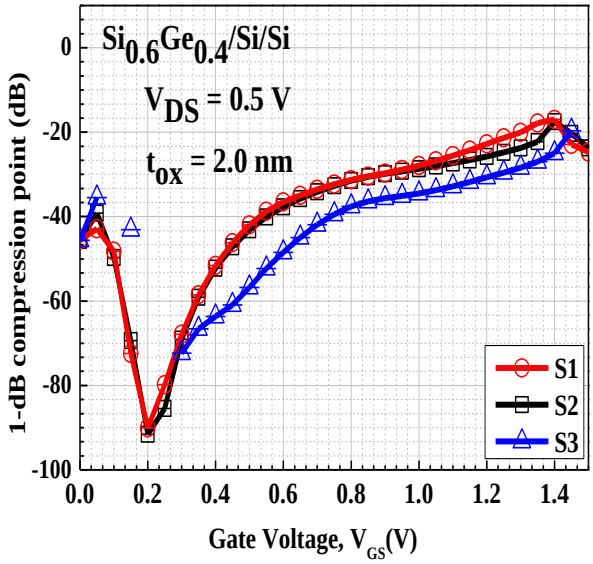
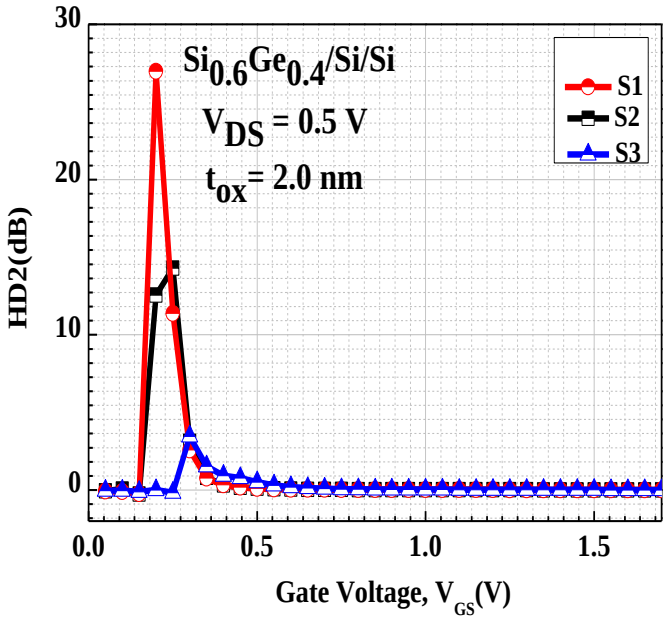



Fig.14: Variation of 1-db compression point with respect to applied gate voltage

In order to understand the harmonic distortion (HD) characteristics of devices, the second - order HD (i.e., HD2) and third - order HD (i.e., HD3) are measured from the approximate analytical expression given by Equation(16) [29-30]. In the present study, the amplitude of input sinusoidal (Va) is considered to be very small and HD2 and HD3 is determined by $g_m$ and its first and second-order derivative [30] respectively. Fig. 15 shows the variation in HD2, HD3, with $V_{GS}$ and constant temperature, T=300K respectively. From this figure, it is analyses that, the structure S1 has slightly larger HD. It has also been observed that the topologies, geometry and the choice of the position of the oxides influence the tunnel phenomenon, resulting the distortion parameters HD2 and HD3 which are linked to the amplification factor $g_m$ and the inflection points of the curves gm2 and gm3. The S1 structure confirms the best linearity of the system for $V_{DS}$ = 0.5 V for device doping levels for source ($N_S$ =1.1x10$^{20}$/cm$^3$), drain ($N_D$ =5.1x10$^{18}$ /cm$^3$) and channel ($N_C$ =1.1×10$^{15}$ /cm$^3$) respectively. Also, the total harmonic distortion (HD) as given by Equation (17) [30]. The difference in shift of HD3 between structure S1 and S2 is ~ 50 and structure S2 and S3 is ~6x10$^{-3}$dB.The shift of HD2 between structure S1,S2 and S2, S3 is ~10 dB.

$$\begin{cases} HD2 = \frac{1}{2} V_a \frac{\frac{dg_m}{dV_{GS}}}{2g_m} \\ HD3 = \frac{1}{4} {V_a}^2 \frac{\frac{d^2 g_m}{dV^2{}_{GS}}}{6g_m} \end{cases} \qquad (16)$$

$$HD_{Total} = \sqrt{HD2^2 + HD3^2 + \cdots} \qquad (17)$$



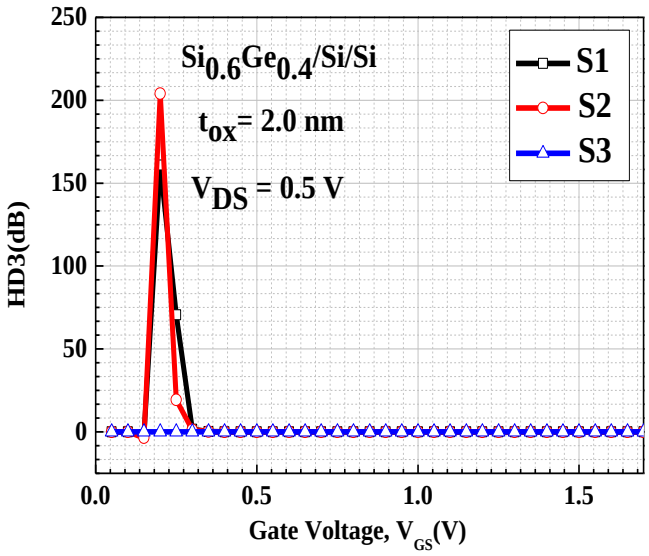



Fig.15: Variation of e second - order HD (i.e., HD2) and third - order HD (i.e., HD3 distortion (HD) characteristics of deviceswith respect to applied gate voltage ($V_{GS}$)

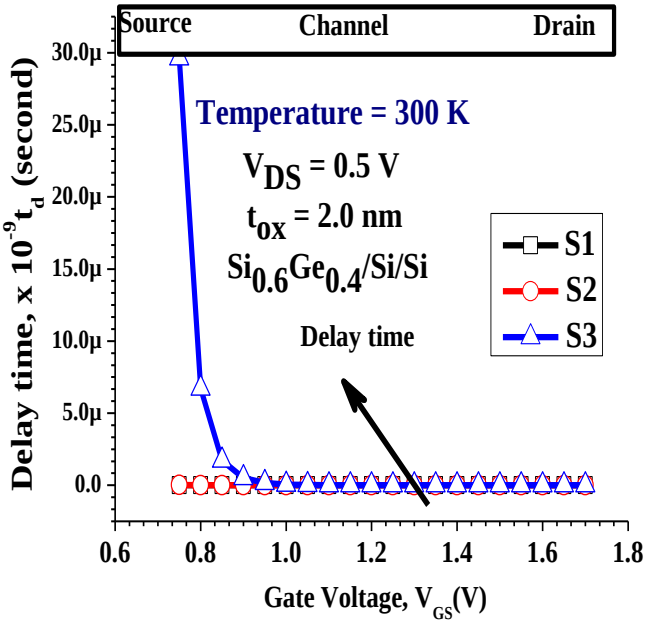



Fig. 16.: Propagation delay variation with applied gate voltage, $V_{GS}$

Fig. 16 shows the delay time ($\iota_D$) versus gate applied voltage, following Equation (18). From Fig. 16, it could be observed that the delay time is bias weak dependent. That is to say that the decrement rate of the gate voltage $V_{GS}$ with hetero gate double DG-Tunnel FET with smaller delay time than homo structure DG-TFET. As shown in Fig.16, the response time of structure S3 is larger than S1 and S2.

$$\tau_D = \frac{1}{2\pi f_T} \qquad (18)$$

Fig. 17 predicts increased power delay product (PDP) with $V_{GS}$ analysis of designed Tunnel FET structures. It is should be noted that, the power delay product is bias-dependent. It strongly depends on input voltage $V_{GS}$.The analysis results revel that structure S1 having larger values of PDP, while is more sensitive with applied input signal.

Fig. 18 shows deviation of design matrix elements. In structure S1, it has been noticed an improvement performance in term of $V_{th}$ (≈ 0.3%), $I_{ON}$ (≈ $1.03\times10^{-3}$A/μm), $I_{ON}/I_{OFF}$ ratio (≈ $10^{13}$), $f_T$ (≈ 60.92%) and GBW (≈ 6.92%). This is due to better electrostatic performance than other designed structures. The difference shift of HD3 between S1/S2 is about 50dB and S2/S3 is about $6x10^{-3}$ dB and a shift of HD2 between S1/S2 and S2/S3 is about 100V. In summary, the analog/RF circuit and system design metrics elements such as VIP2, VIP3, IMD3 and IIP3 are better for device S1, shown in Fig.1 as compared to S2 and S3. The 1- dB compression point is higher than other S2 and S3. When TFET device S1 is used in circuit level on weak signal, less in termoduction distortion (IMDs) that lead to unwanted distorted signal in the output as compared to the input signals [26], thus IMD should be minimum. It is shown that symmetric high- k, staggered DG - Tunnel FET is more linear than asymmetric configuration counterpart and linearity can improved by careful optimization of device configuration. For deviation of design matrix elements for designed structures, the data analysis with the help or Origin software, and the results are shown in Fig.18.

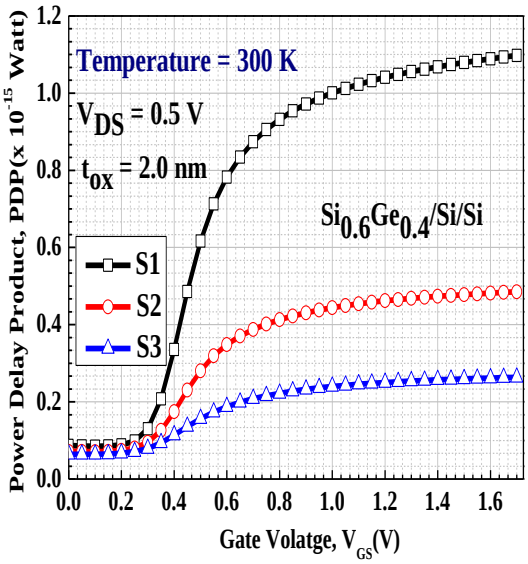



Fig. 17.: Power delay product variation with applied gate voltage, $V_{GS}$

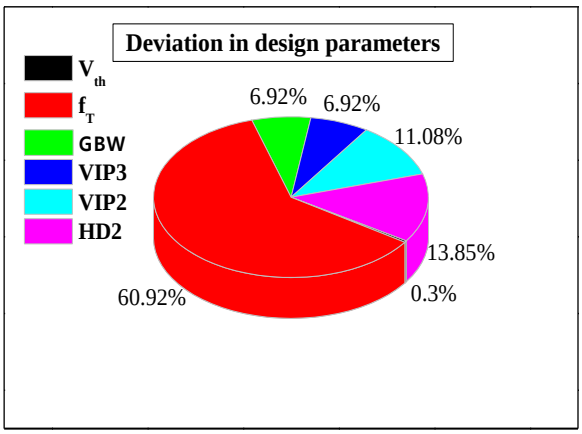



Fig. 18.: Deviation (i.e., % change) in design circuit parameter in proposed device structure

## 4. CONCLUSION

In summary, a comprehensive investigation of the proposed Tunnel FET structures for low power analog /RF circuit design applications have been presented in this article. The reported investigation reveals that $g_m$ of Tunnel FET is slightly smaller than conventional MOSFET, due to band-to-band tunnelling. The designed tunnel FET structure (s1) containing hetero source/ channel ($SI_{1-X}GE_X$ /SI) with only homo gate dielectric $HFO_2$( k≈ 25) shows the optimum design matrix element in terms $i_{on}$(≈$1.03\times10^{-3}$a/µm), $i_{off}$(≈$1.31\times10^{-17}$a/µm), $i_{on}/i_{off}$( ≈ $10^{13}$) and and transconductance($g_m$). the cutoff frequency ($f_t$)of tunnel fet is commonly lesser conventional mosfet due to lower $i_{on}$and its derivative $g_m$.the smaller$f_t$values limit its use at very high frequency(rf) applications. the worldwide effort for improvement of $i_{ds}$ is continue to improve its dependent design elements such $g_{m,t}$ and gain band width (gbw). due to incorporation of gate dielectric engineering and staggered source, channel configuration provides significant improvement in $i_{on}$ current. the analysis results show, structure s1 has superior performance in terms of design matrix elements such as tgf, vip2, vip3, imd3, iip3, 1- db compression point and optimum harmonic distortions (hd2 and hd3).the delay and power delay product (pdp) performance analysis of designed tunnel fet structures reveals that the gate dielectric engineering technique plays a crucial factor for boosting the device performance in terms of modern ultra-low power applications such as for the IOT and wearable electronics. Our investigation proves that tunnel FET is a strong candidate for replacement of conventional mosfet for analog/rf applications with moderate frequencies and low power applications.

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